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# MS-7982V21

## CPU:

**SKYLAKE-S**

## System Chipset:

**B150**

## SIO:

**NTC6793D**

## VRM:

**RT3606BC**

## Onboard Chip:

**LAN-RT8111H**

**Audio-ALC887**

## Main Memory:

**DDRIII (800/1066/1333MHz) \* 4**

## Expansion Slots:

**PCI Express (X16) Slot x1**

**PCI Express (X1 ) Slot x2**

## Other:

**SATAE x1**

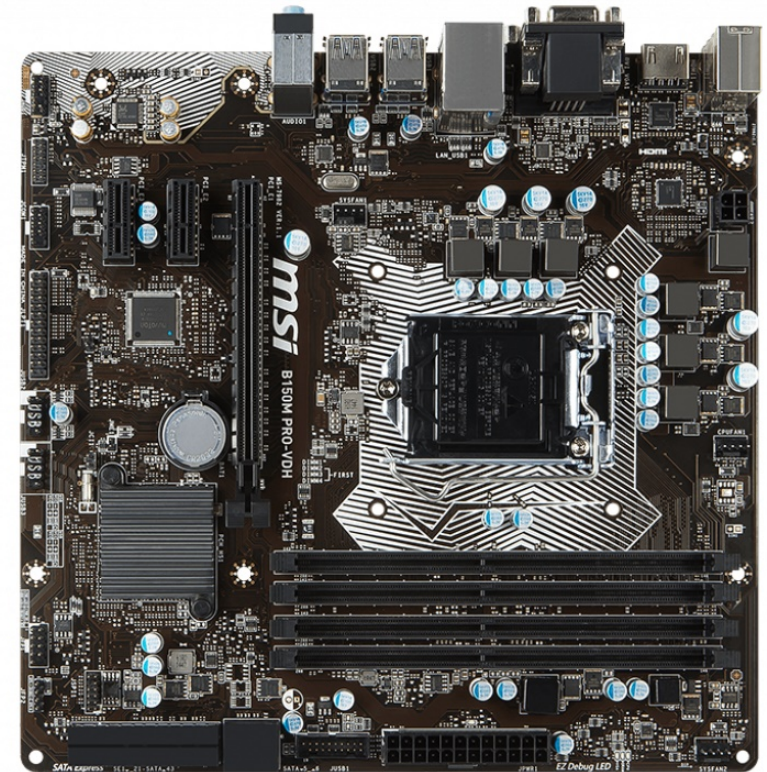
**SATA3.0 x4**

**REAR USB2.0 x2**

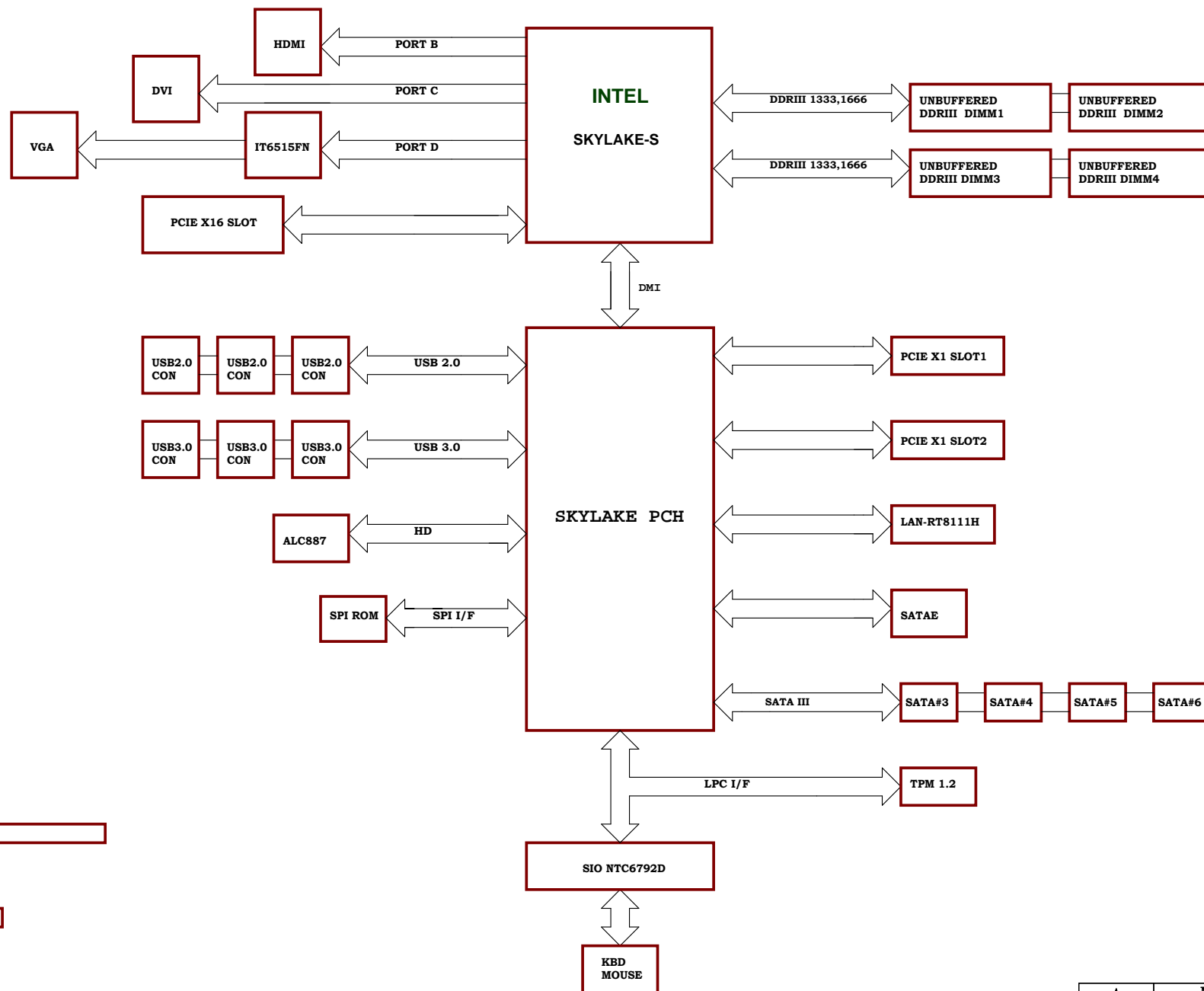
**REAL USB3.0 x4**

**FRONT USB2.0 x4**

**FRONT USB3.0 x2**



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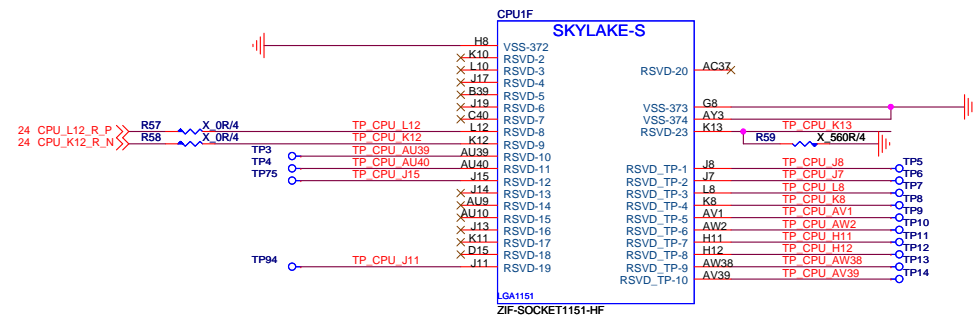
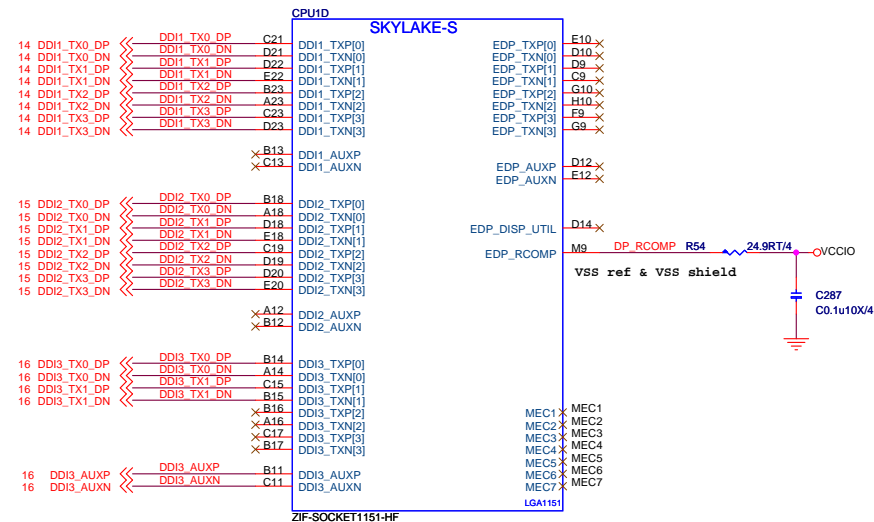
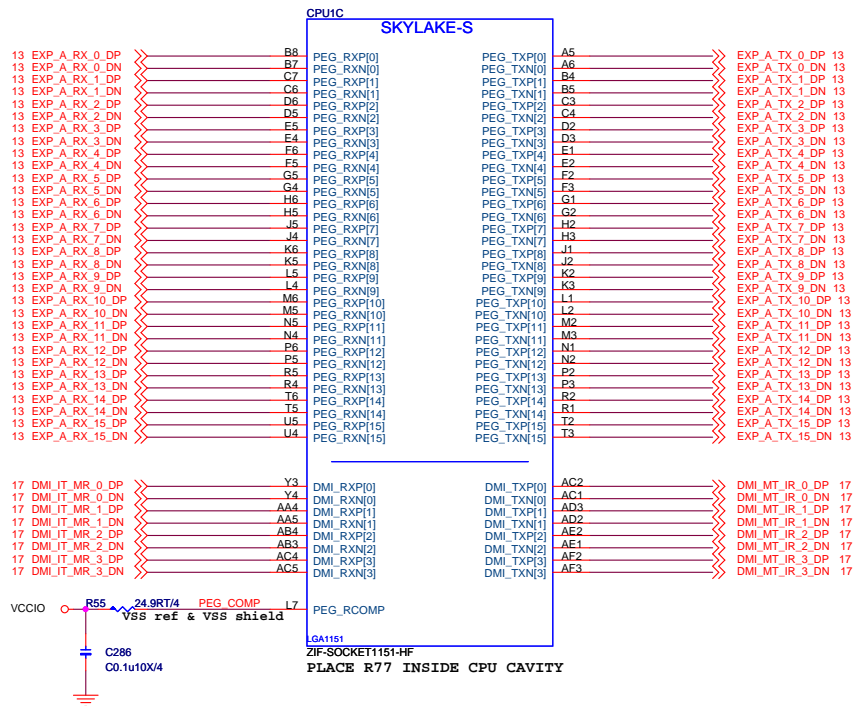


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10 M\_DATA\_B[63:0] <<> M\_DATA\_B[63:0]

CPU1B

SKYLAKE-S

M\_DATA\_B0 AD34  
M\_DATA\_B1 AD35  
M\_DATA\_B2 AG35  
M\_DATA\_B3 AH35  
M\_DATA\_B4 AE35  
M\_DATA\_B5 AE34  
M\_DATA\_B6 AG34  
M\_DATA\_B7 AH34  
M\_DATA\_B8 AK35  
M\_DATA\_B9 AK35  
M\_DATA\_B10 AK32  
M\_DATA\_B11 AL32  
M\_DATA\_B12 AK34  
M\_DATA\_B13 AL34  
M\_DATA\_B14 AK31  
M\_DATA\_B15 AL31  
M\_DATA\_B16 AP35  
M\_DATA\_B17 AN35  
M\_DATA\_B18 AN32  
M\_DATA\_B19 AP32  
M\_DATA\_B20 AN34  
M\_DATA\_B21 AP34  
M\_DATA\_B22 AN31  
M\_DATA\_B23 AP31  
M\_DATA\_B24 AL29  
M\_DATA\_B25 AM29  
M\_DATA\_B26 AP29  
M\_DATA\_B27 AM29  
M\_DATA\_B28 AR29  
M\_DATA\_B29 AL28  
M\_DATA\_B30 AR28  
M\_DATA\_B31 AR28  
M\_DATA\_B32 AR12  
M\_DATA\_B33 AP12  
M\_DATA\_B34 AM13  
M\_DATA\_B35 AL13  
M\_DATA\_B36 AR13  
M\_DATA\_B37 AP13  
M\_DATA\_B38 AM12  
M\_DATA\_B39 AL12  
M\_DATA\_B40 AP10  
M\_DATA\_B41 AR10  
M\_DATA\_B42 AR7  
M\_DATA\_B43 AP7  
M\_DATA\_B44 AR9  
M\_DATA\_B45 AP9  
M\_DATA\_B46 AR6  
M\_DATA\_B47 AP6  
M\_DATA\_B48 AM10  
M\_DATA\_B49 AL10  
M\_DATA\_B50 AM7  
M\_DATA\_B51 AL7  
M\_DATA\_B52 AM9  
M\_DATA\_B53 AL9  
M\_DATA\_B54 AM6  
M\_DATA\_B55 AL6  
M\_DATA\_B56 AJ6  
M\_DATA\_B57 AJ7  
M\_DATA\_B58 AE6  
M\_DATA\_B59 AE7  
M\_DATA\_B60 AH7  
M\_DATA\_B61 AH6  
M\_DATA\_B62 AE7  
M\_DATA\_B63 AF6

DDR0\_DQ[16]/DDR1\_DQ[0]  
DDR0\_DQ[17]/DDR1\_DQ[1]  
DDR0\_DQ[18]/DDR1\_DQ[2]  
DDR0\_DQ[19]/DDR1\_DQ[3]  
DDR0\_DQ[20]/DDR1\_DQ[4]  
DDR0\_DQ[21]/DDR1\_DQ[5]  
DDR0\_DQ[22]/DDR1\_DQ[6]  
DDR0\_DQ[23]/DDR1\_DQ[7]  
DDR0\_DQ[24]/DDR1\_DQ[8]  
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DDR1\_DQ[30]/DDR1\_DQ[46]  
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DDR1\_DQ[57]  
DDR1\_DQ[58]  
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DDR1\_DQ[60]  
DDR1\_DQ[61]  
DDR1\_DQ[62]  
DDR1\_DQ[63]

DDR1\_MA[0]/DDR1\_CAB[9]/DDR1\_MA[0]  
DDR1\_MA[1]/DDR1\_CAB[8]/DDR1\_MA[1]  
DDR1\_MA[2]/DDR1\_CAB[5]/DDR1\_MA[2]  
DDR1\_MA[3]  
DDR1\_MA[4]  
DDR1\_MA[5]/DDR1\_CAA[0]/DDR1\_MA[5]  
DDR1\_MA[6]/DDR1\_CAA[2]/DDR1\_MA[6]  
DDR1\_MA[7]/DDR1\_CAA[4]/DDR1\_MA[7]  
DDR1\_MA[8]/DDR1\_CAA[3]/DDR1\_MA[8]  
DDR1\_MA[9]/DDR1\_CAA[1]/DDR1\_MA[9]  
DDR1\_MA[10]/DDR1\_CAB[7]/DDR1\_MA[10]  
DDR1\_MA[11]/DDR1\_CAA[7]/DDR1\_MA[11]  
DDR1\_MA[12]/DDR1\_CAB[6]/DDR1\_MA[12]  
DDR1\_MA[13]/DDR1\_CAB[0]/DDR1\_MA[13]  
DDR1\_MA[14]/DDR1\_CAB[2]/DDR1\_WE#  
DDR1\_MA[15]/DDR1\_CAB[1]/DDR1\_CAS#  
DDR1\_MA[16]/DDR1\_CAB[3]/DDR1\_RAS#

DDR1\_BG[1]/DDR1\_CAA[9]/DDR1\_MA[14]  
DDR1\_ACT#/DDR1\_CAA[8]/DDR1\_MA[15]

DDR1\_CKE[0]  
DDR1\_CKE[1]  
DDR1\_CKE[2]  
DDR1\_CKE[3]

DDR1\_CS#0  
DDR1\_CS#1  
DDR1\_CS#2  
DDR1\_CS#3

DDR1\_ODT[0]  
DDR1\_ODT[1]  
DDR1\_ODT[2]  
DDR1\_ODT[3]

DDR1\_BA[0]/DDR1\_CAB[4]/DDR1\_BA[0]  
DDR1\_BA[1]/DDR1\_CAB[6]/DDR1\_BA[1]  
DDR1\_BG[0]/DDR1\_CAA[5]/DDR1\_BA[2]

DDR1\_CKP[0]  
DDR1\_CKN[0]  
DDR1\_CKP[1]  
DDR1\_CKN[1]  
DDR1\_CKP[2]  
DDR1\_CKN[2]  
DDR1\_CKP[3]  
DDR1\_CKN[3]

DDR1\_PAR  
DDR1\_ALERT#

DDR1\_ECC[0]  
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DDR1\_ECC[3]  
DDR1\_ECC[4]  
DDR1\_ECC[5]  
DDR1\_ECC[6]  
DDR1\_ECC[7]

DDR1\_VREF\_DQ

LGA1151

CHANNEL B

ZIF-SOCKET1151-HF

AL19 M MAA\_B0  
AL22 M MAA\_B1  
AM22 M MAA\_B2  
AM23 M MAA\_B3  
AP23 M MAA\_B4  
AL23 M MAA\_B5  
AW26 M MAA\_B6  
AY26 M MAA\_B7  
AU26 M MAA\_B8  
AW27 M MAA\_B9  
AP18 M MAA\_B10  
AU27 M MAA\_B11  
AV27 M MAA\_B12  
AR15 M MAA\_B13  
AL17 M WE\_B\_N  
AP16 M CAS\_B\_N  
AN18 M RAS\_B\_N

AY28 M MAA\_B14  
AU28 M MAA\_B15

AY29 M SCKE\_B0  
AV29 M SCKE\_B1  
AW29 M SCKE\_B2  
AU29 M SCKE\_B3

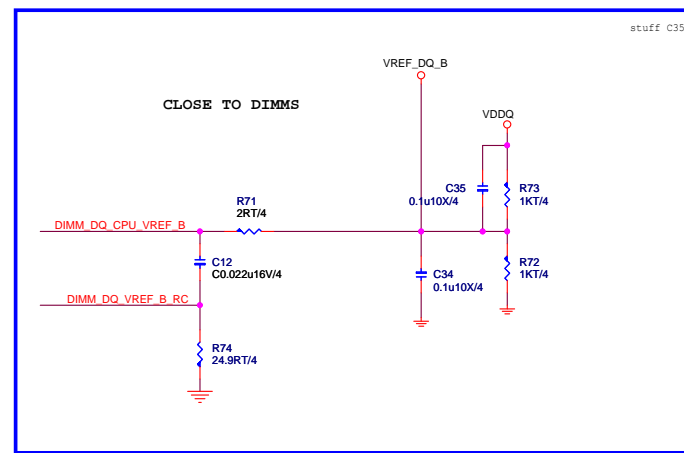
AP17 M SCS\_B\_N0  
AN15 M SCS\_B\_N1  
AN17 M SCS\_B\_N2  
AM15 M SCS\_B\_N3

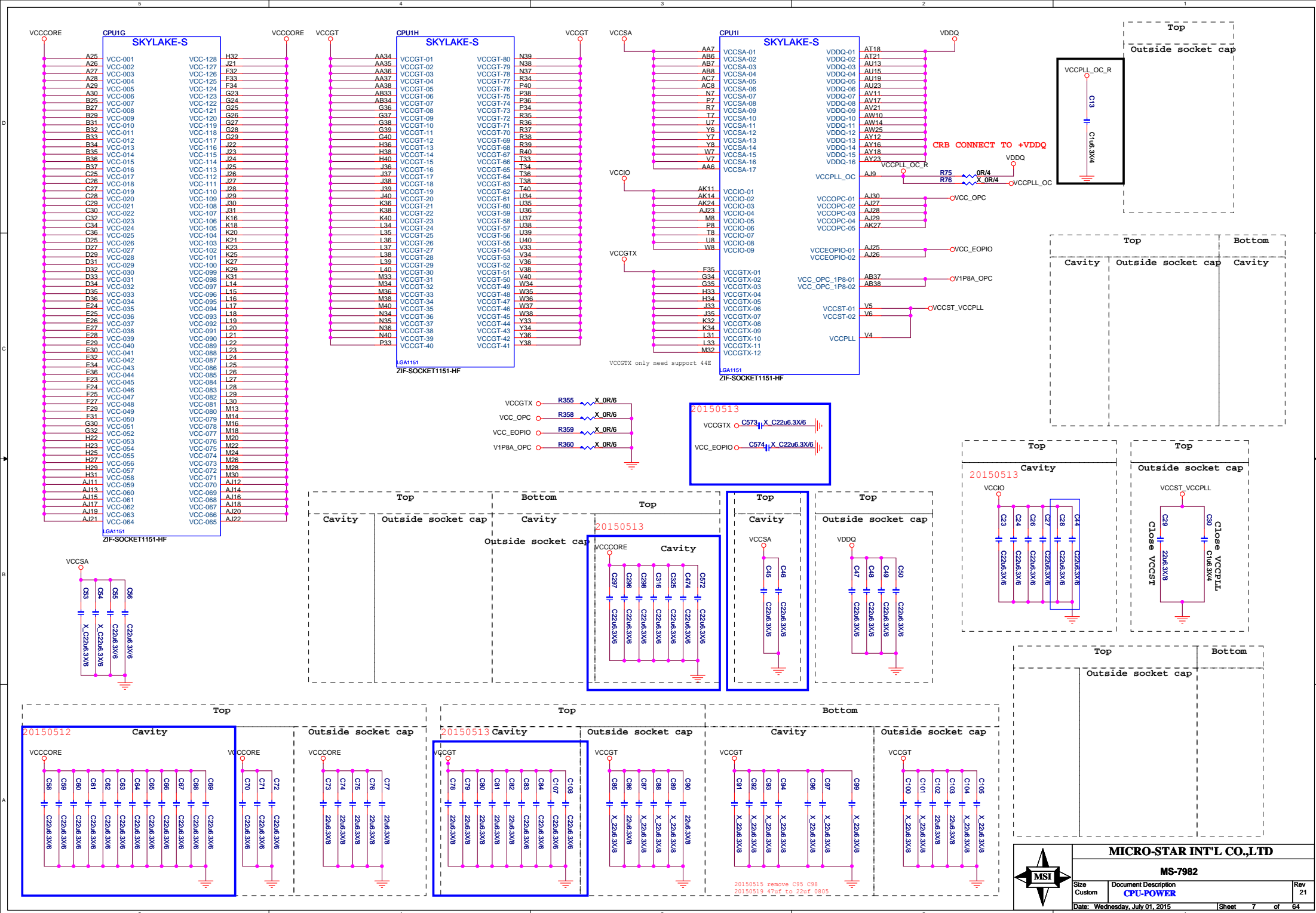
AM16 M ODT\_B0  
AL16 M ODT\_B1  
AP15 M ODT\_B2  
AL15 M ODT\_B3

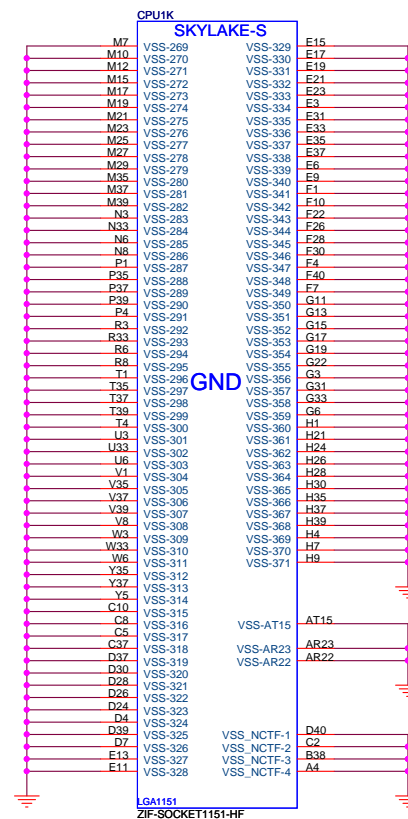
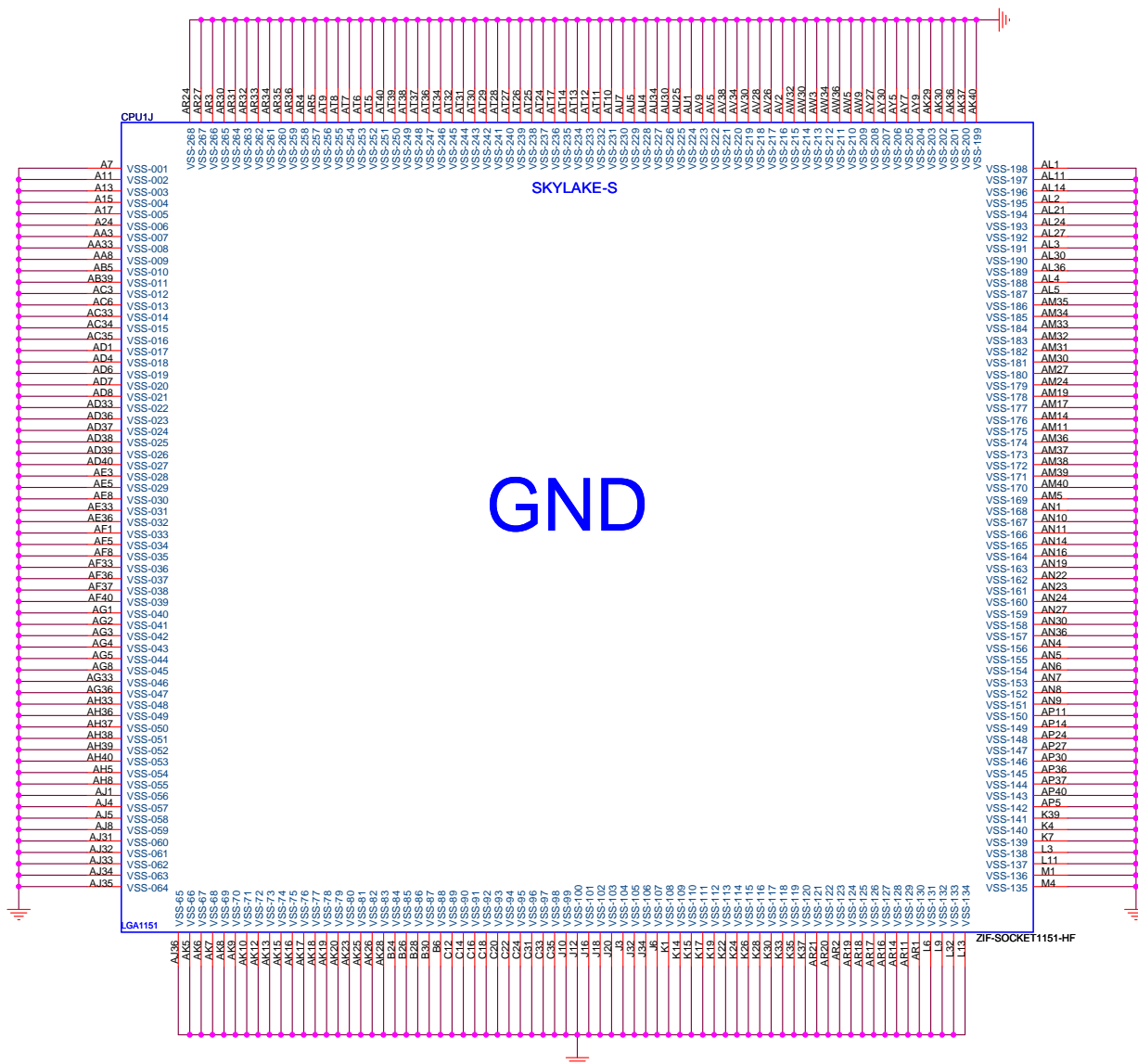
AL18 M SBS\_B0  
AM18 M SBS\_B1  
AW28 M SBS\_B2

AM20 CK M\_DDR0\_B\_DP  
AM21 CK M\_DDR0\_B\_DN  
AP21 CK M\_DDR1\_B\_DP  
AN20 CK M\_DDR2\_B\_DP  
AN21 CK M\_DDR2\_B\_DN  
AP19 CK M\_DDR3\_B\_DP  
AP20 CK M\_DDR3\_B\_DN

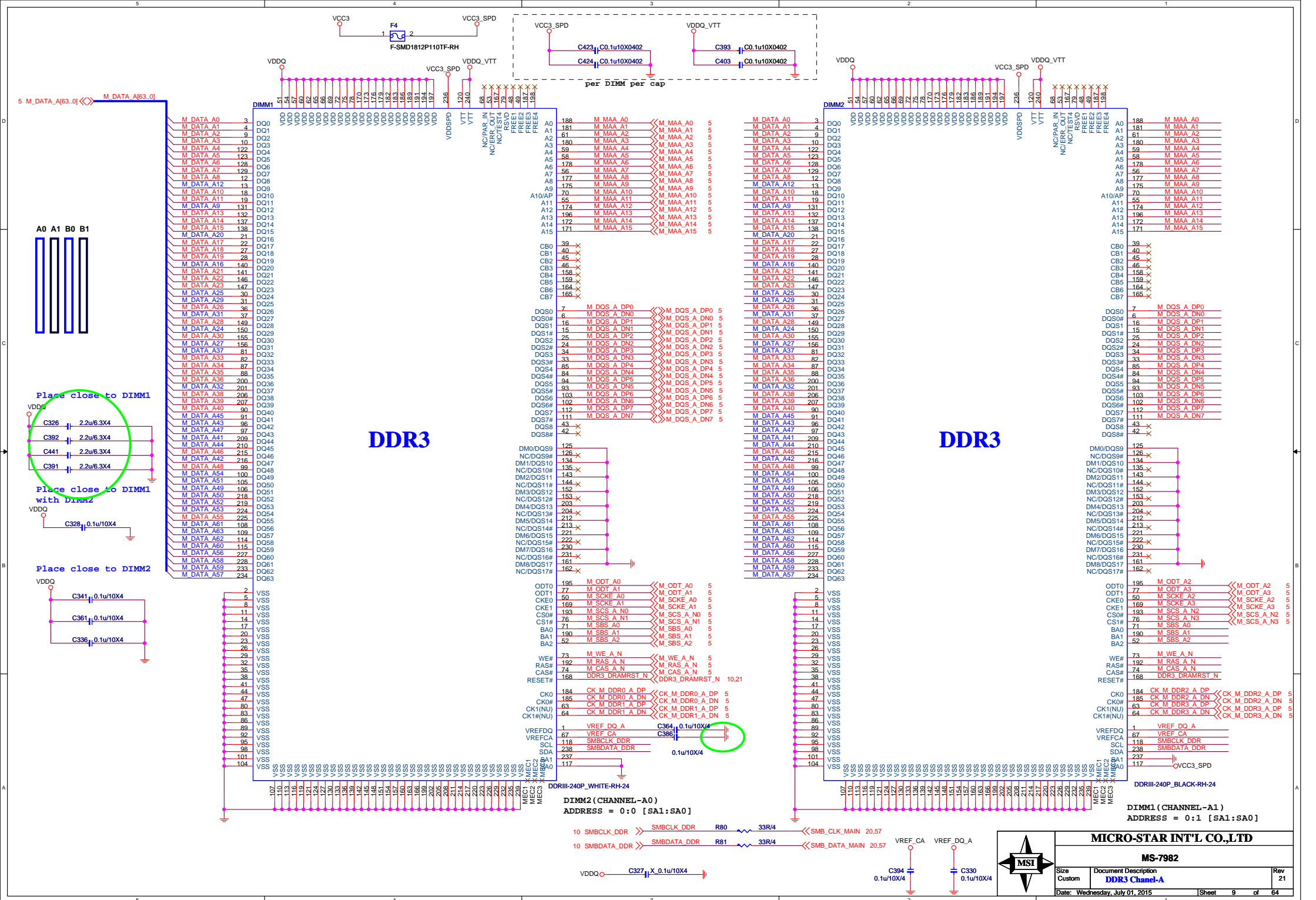
NOTE:CMD SIGNALS FOR DEFERRED MEMORY TECHNOLOGY  
LEFT TO RIGHT: DDR3L/LPDDR3/DDR4



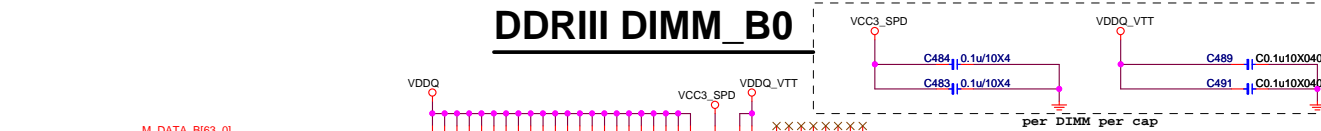




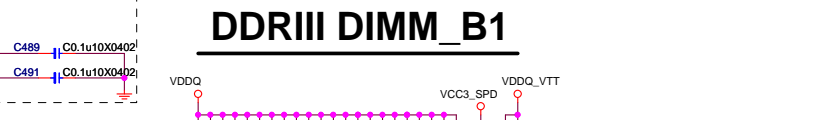




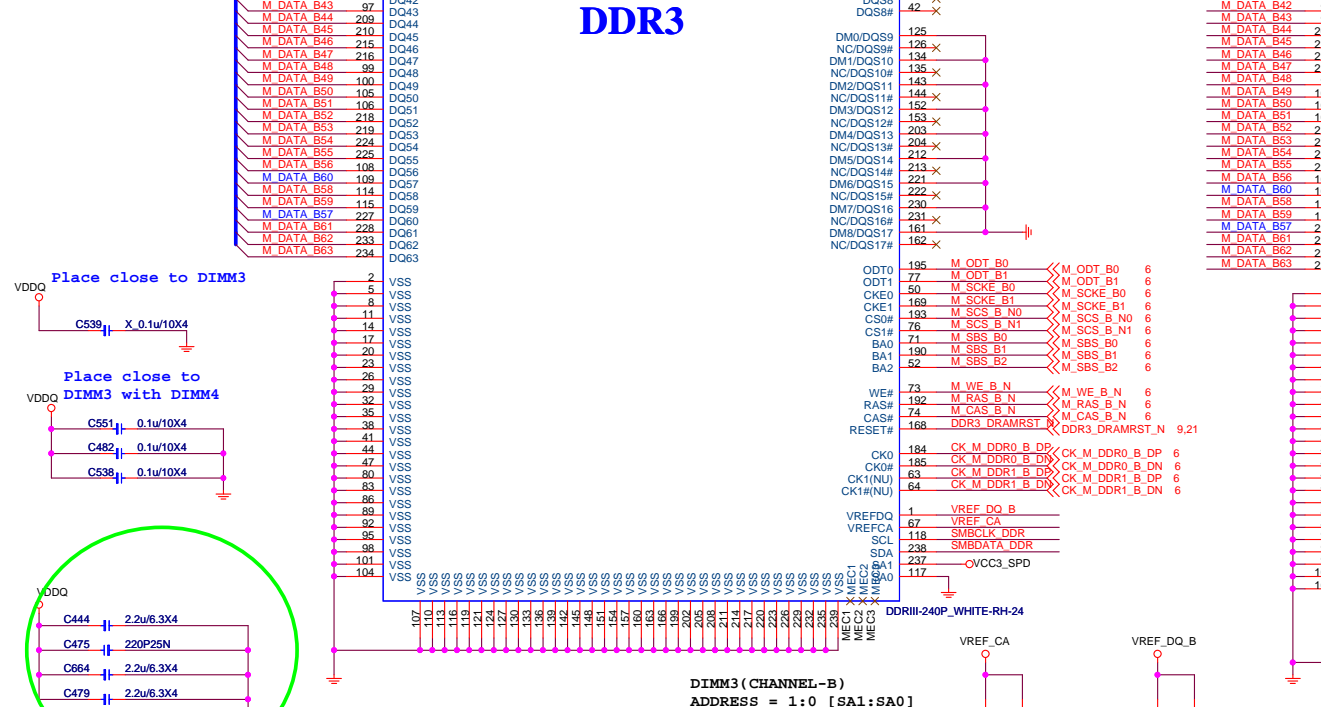
## DDRIII DIMM\_B0



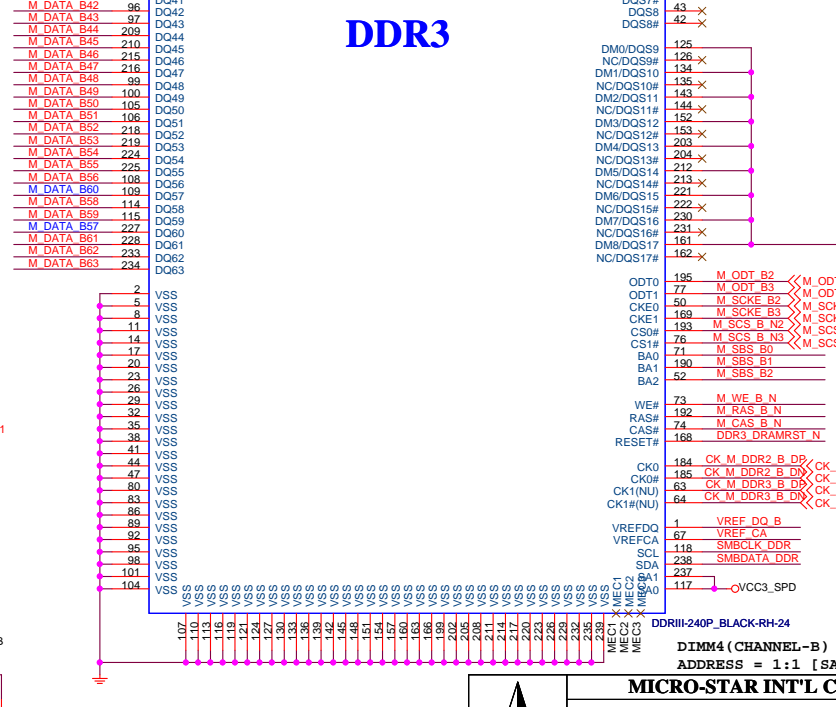
## DDRIII DIMM\_B1



## DDR3



## DDR3

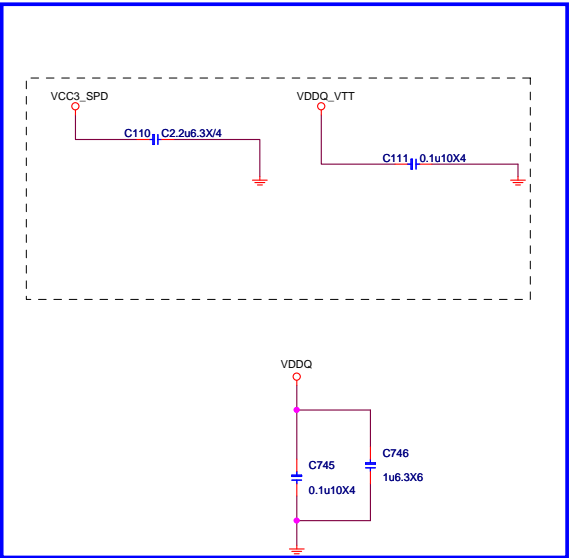
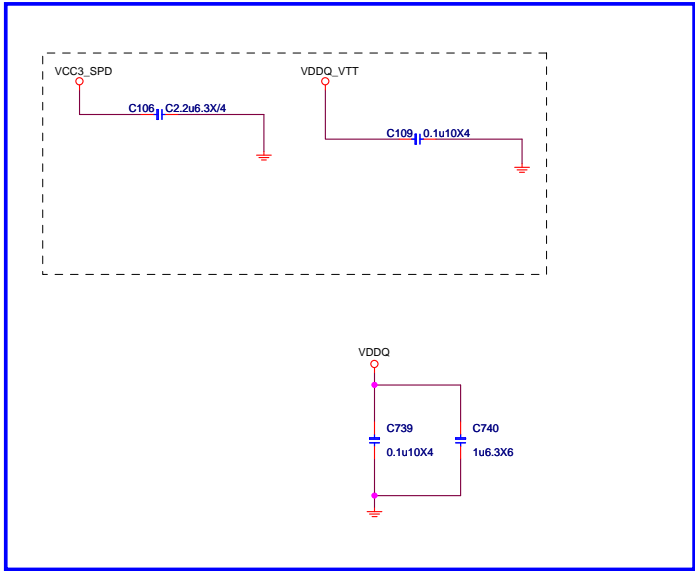


```
MEC DIMM4 ( CHANNEL-B )
MEC ADDRESS = 1:1 [SA1:SA0]
MEC
```

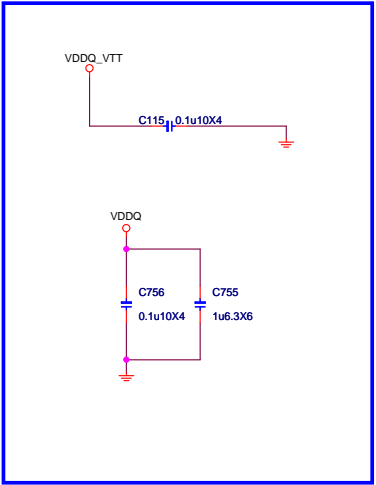
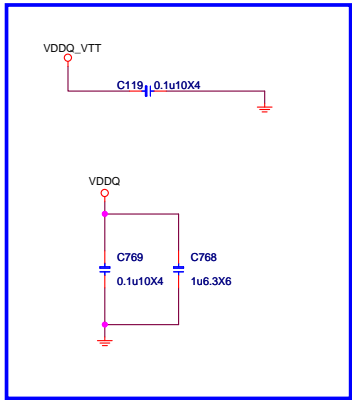
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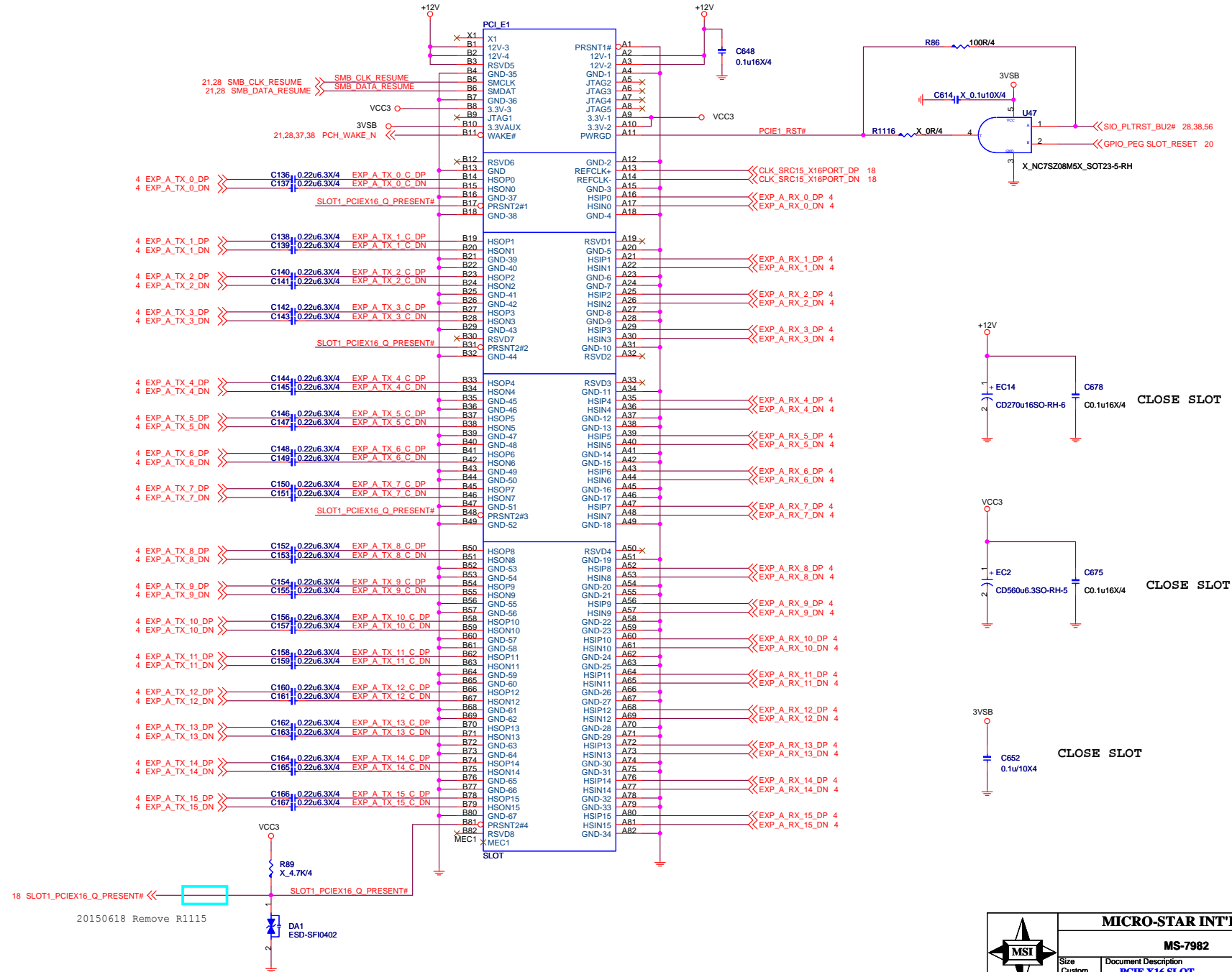


MICRO-STAR INT'L CO.,LTD		
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**PCI\_Express X16 Slot**  
(Share with PCI\_E x8 Slot)

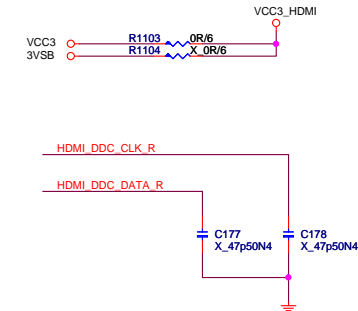
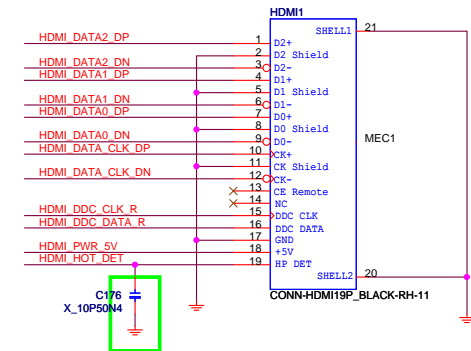
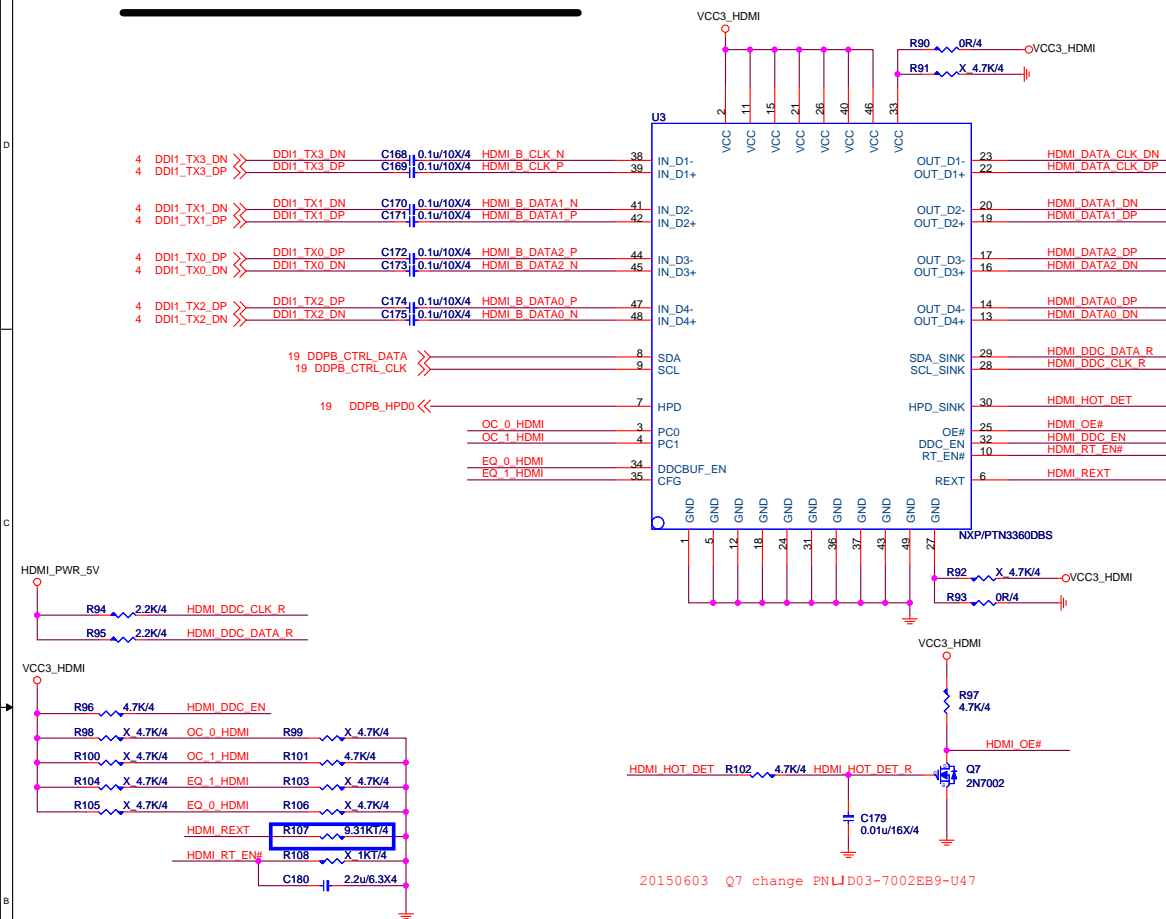


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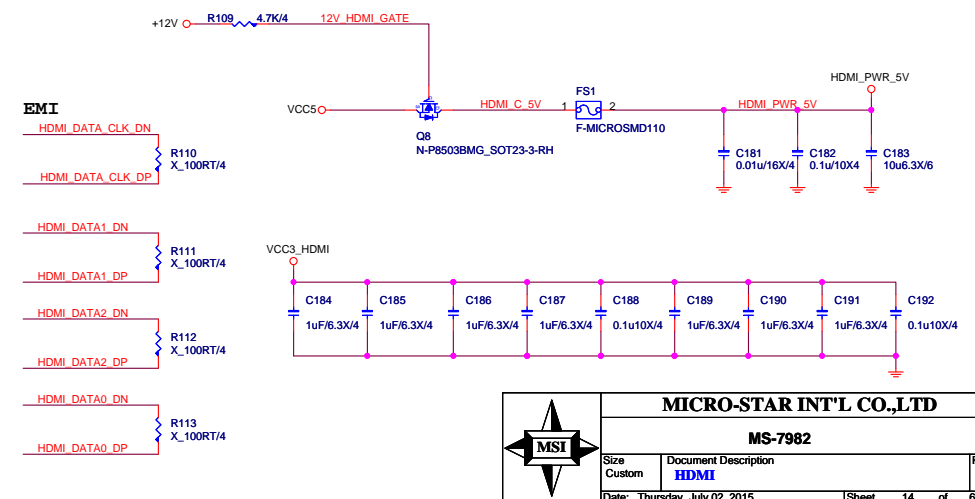
Size Custom	Document Description <b>PCIE X16 SLOT</b>	Rev 21
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## HDMI level shifter



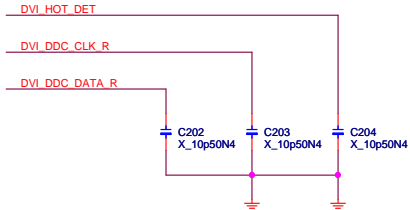
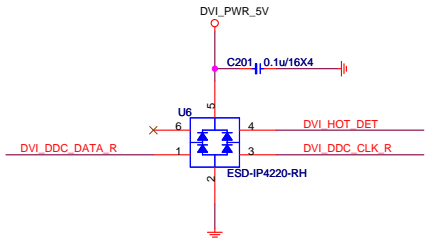
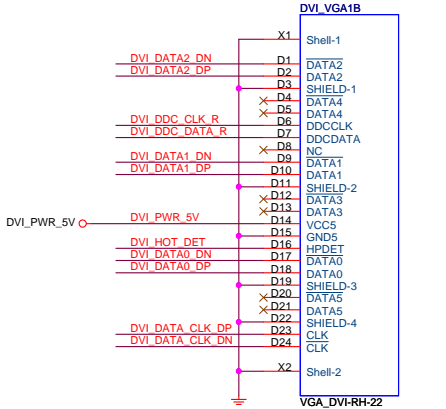
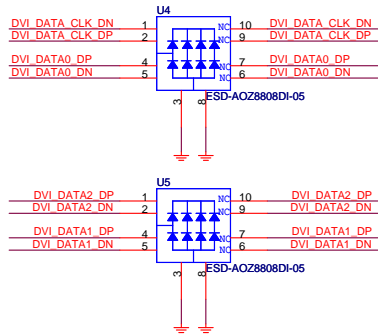
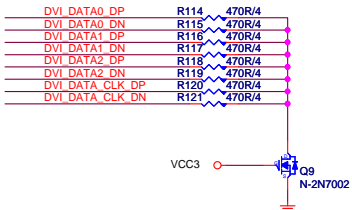
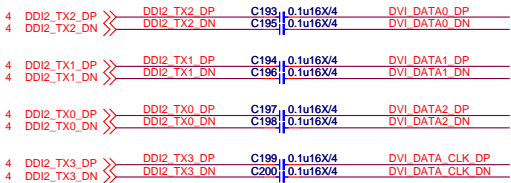
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current

			generation.		
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer	PCI, PC0		note
1, 0, X	On	Off	00	8 dB	internal pull-down at ~500K ohm.
1, 1, 0	Off	On	01	4 dB	
1, 1, 1	Off	Off	10	12 dB	
0, X, X	Off	Off	11	0 dB	

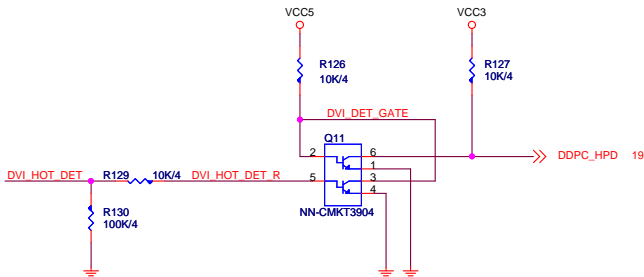




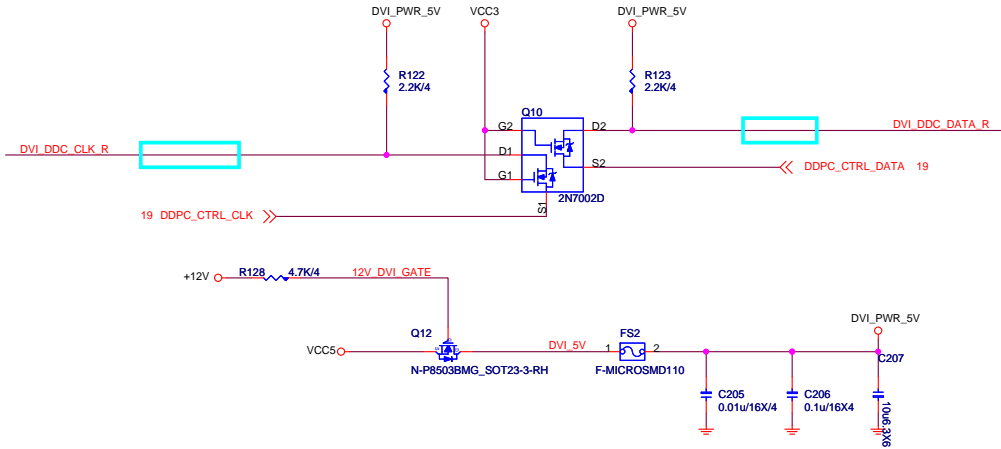
DVI level shifter



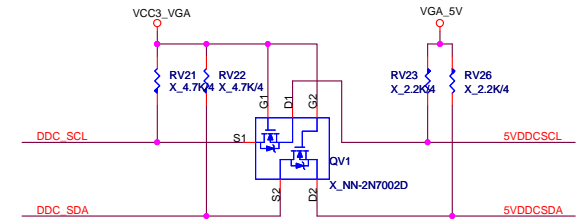
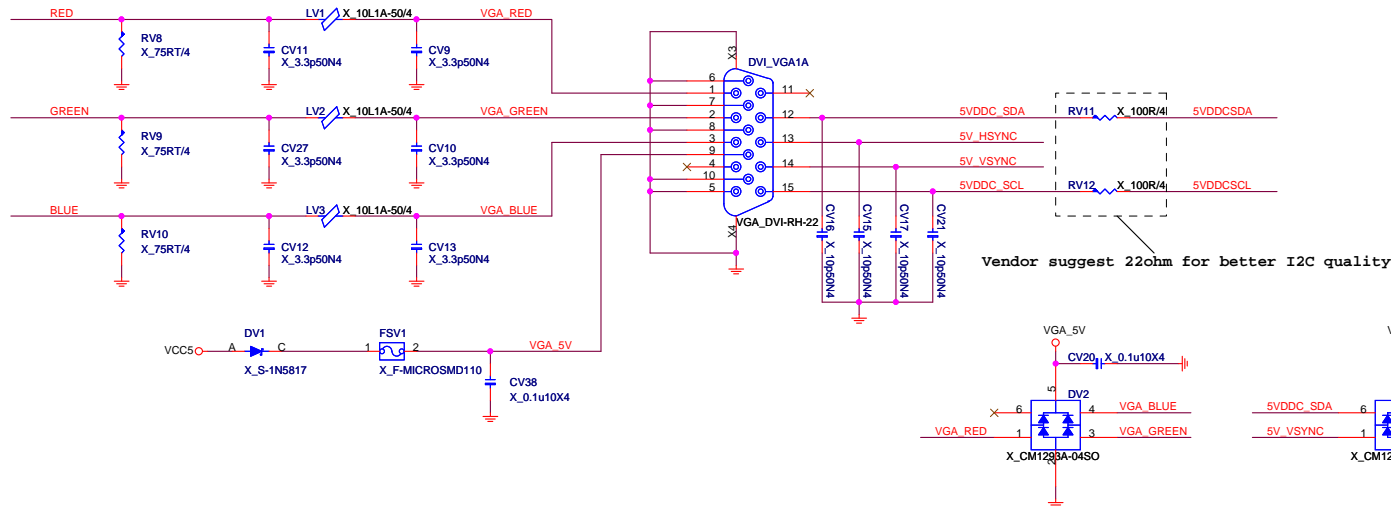
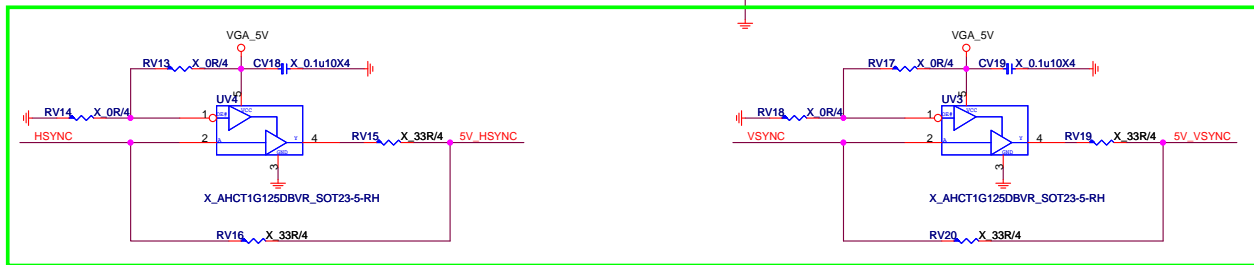
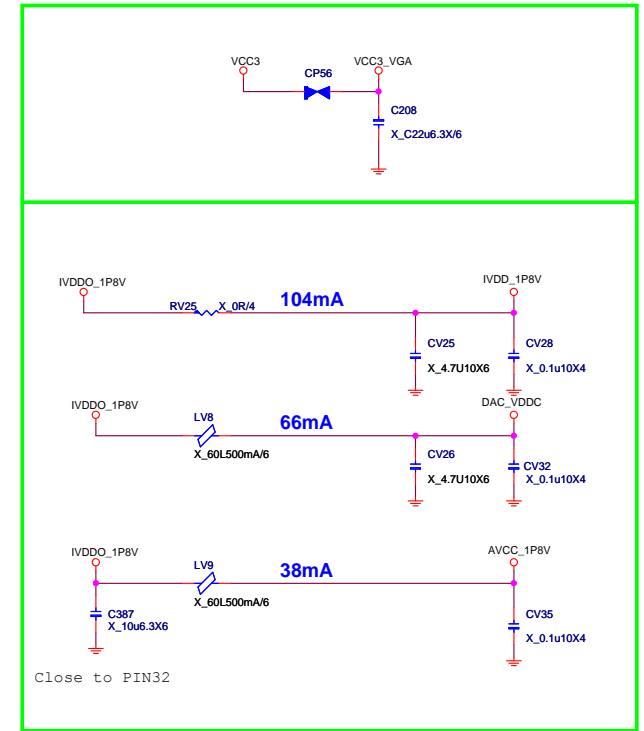
HPD



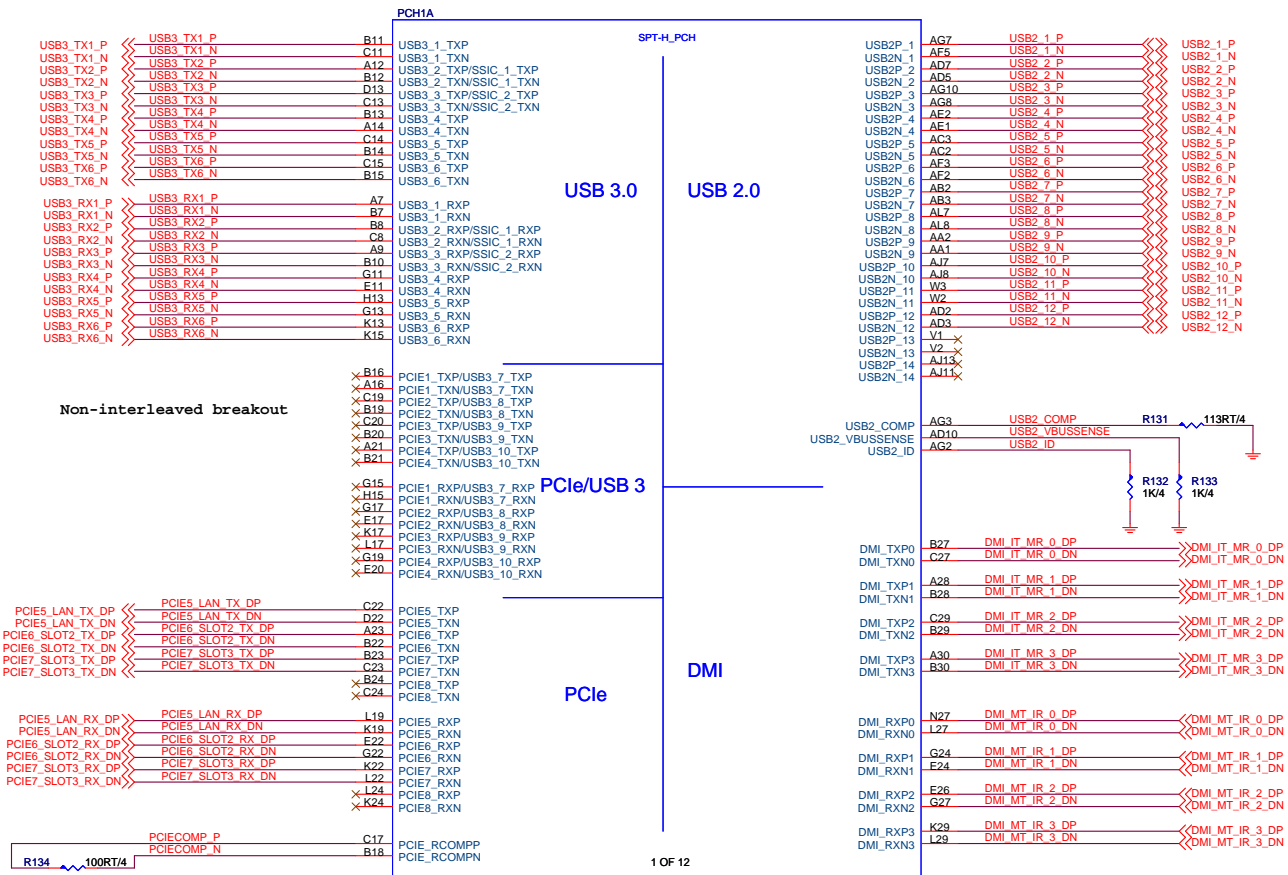
20150624 remove R125 R124

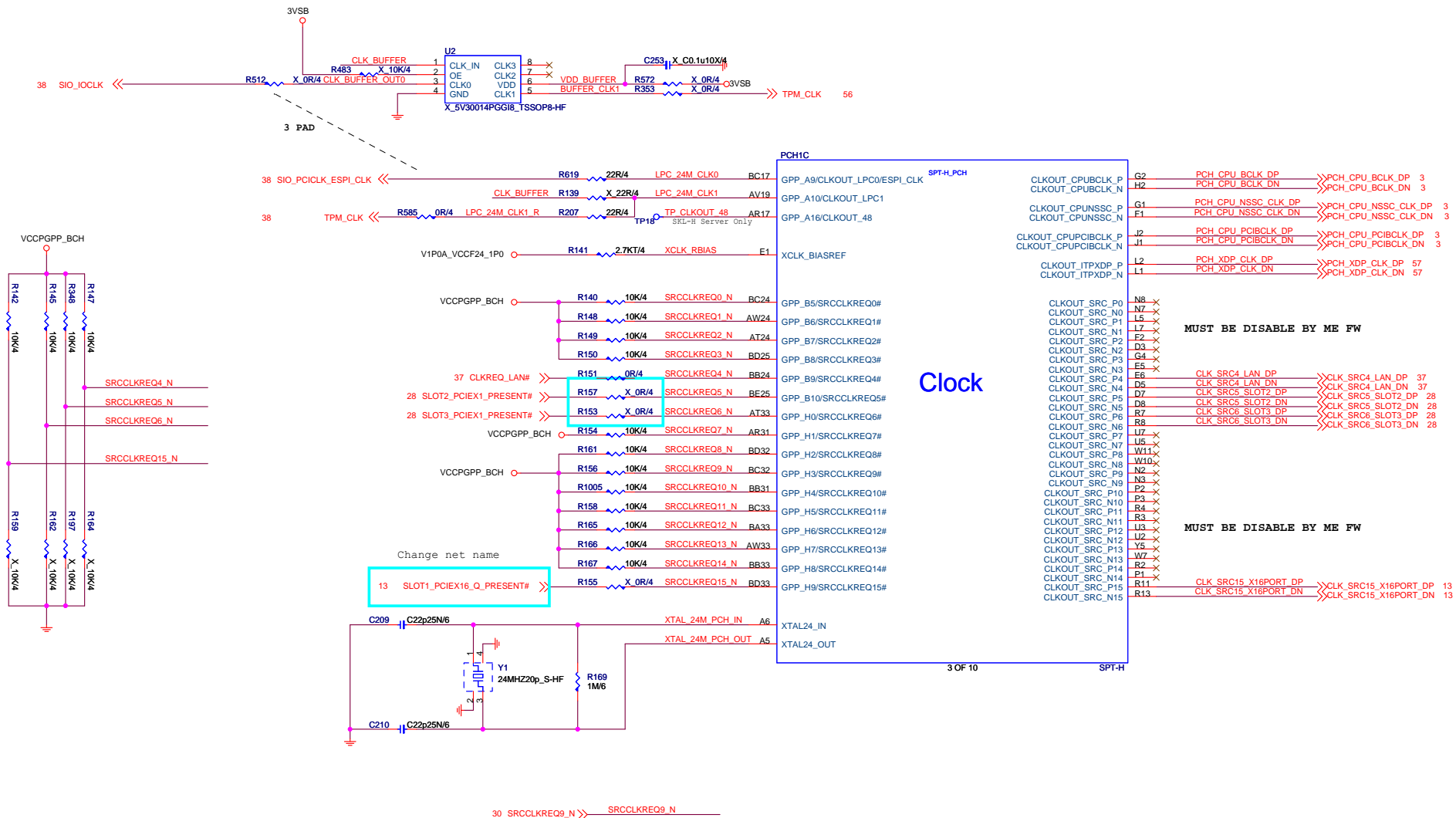


If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



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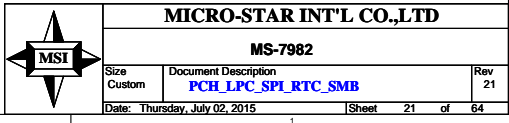




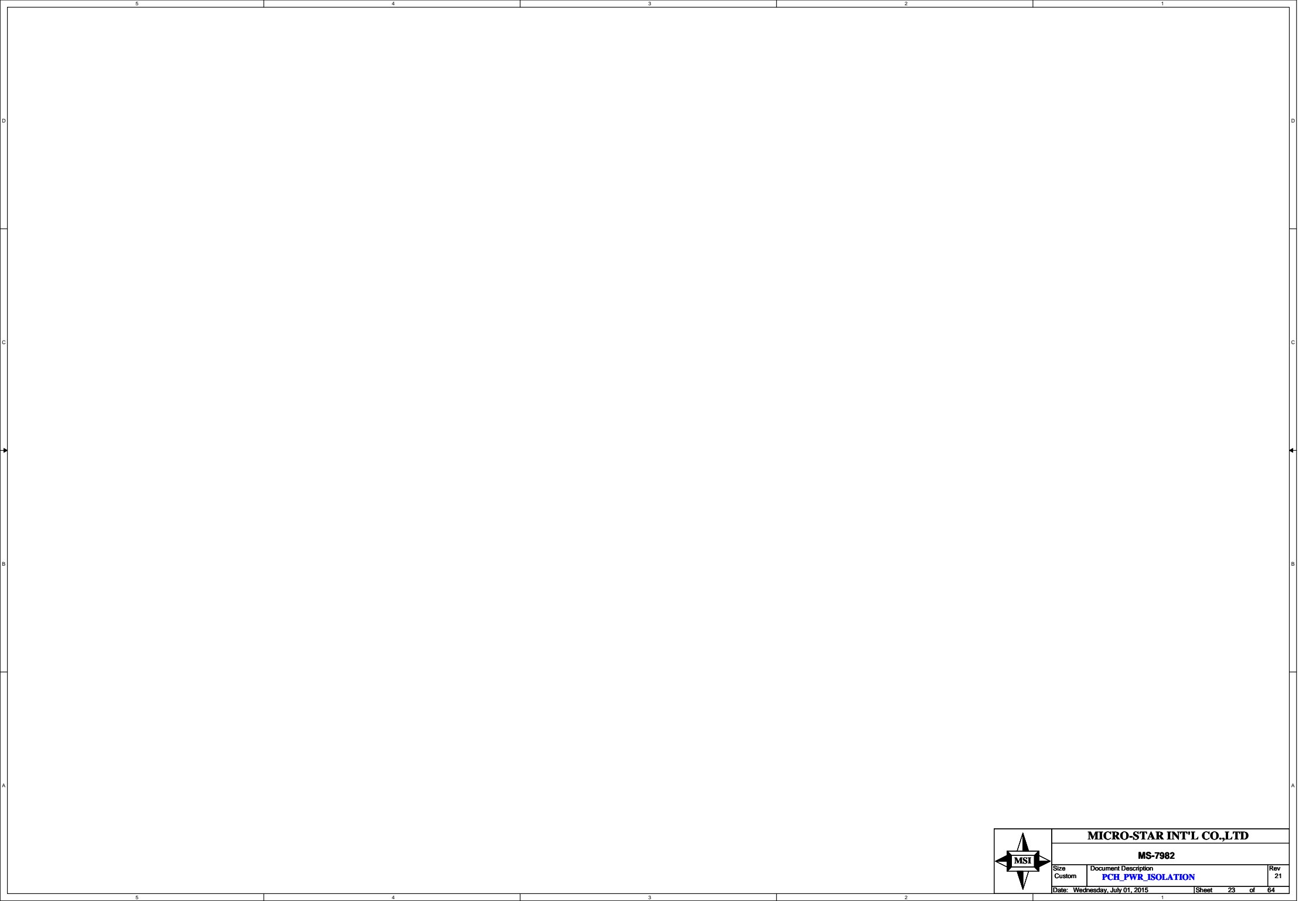










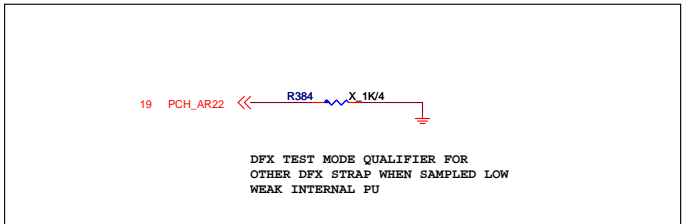
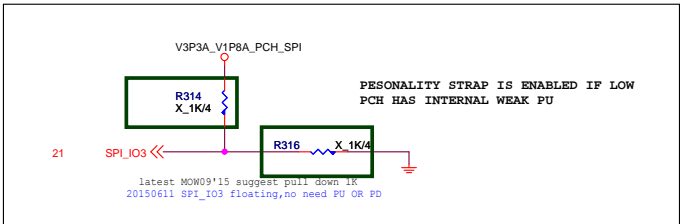
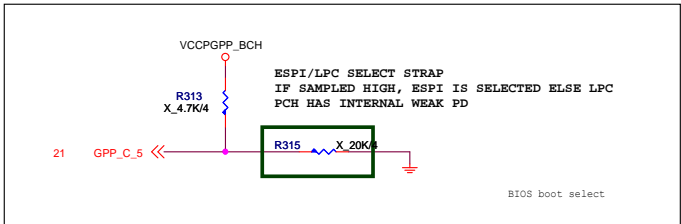
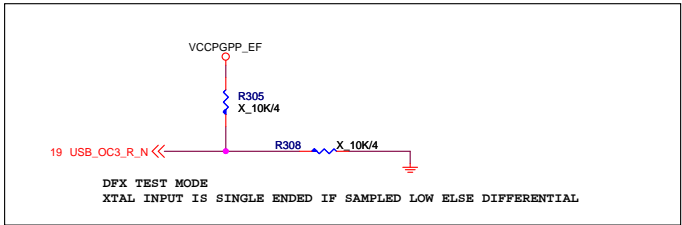
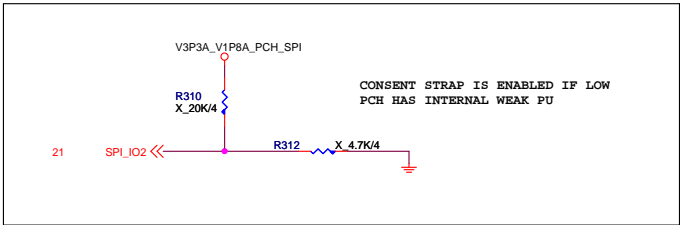
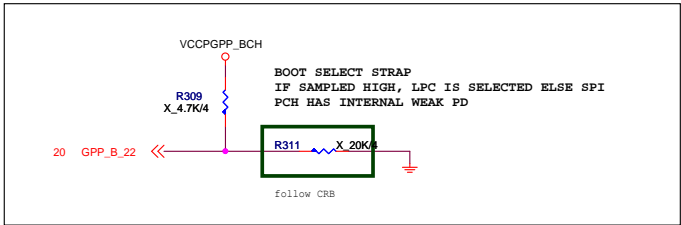
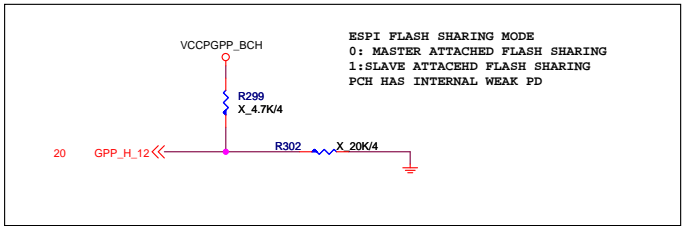
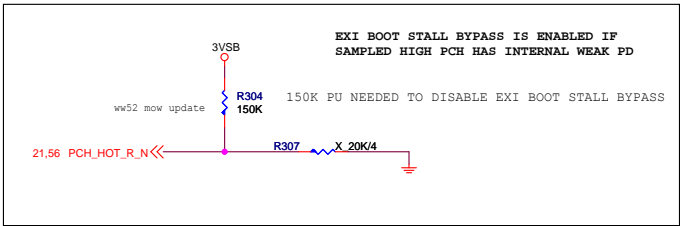
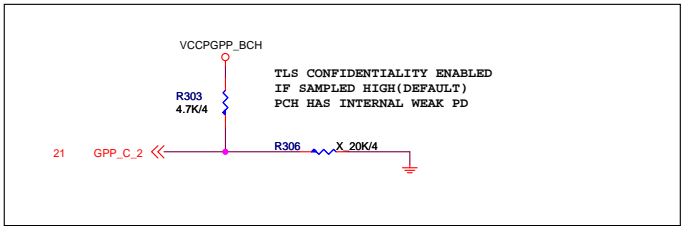
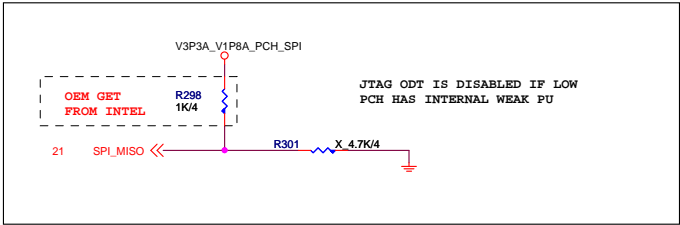
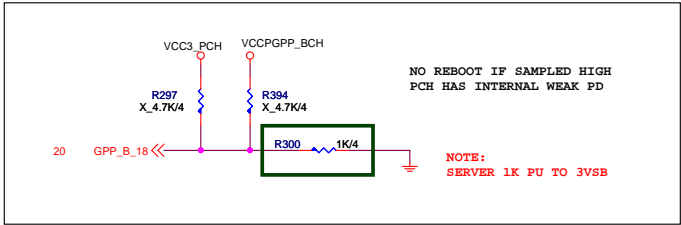
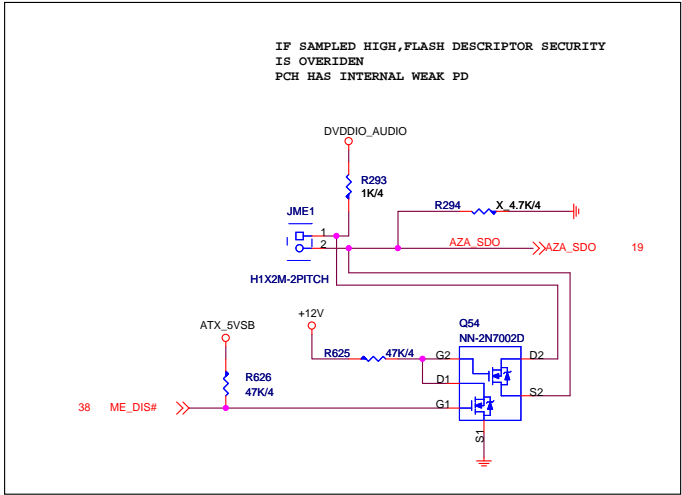
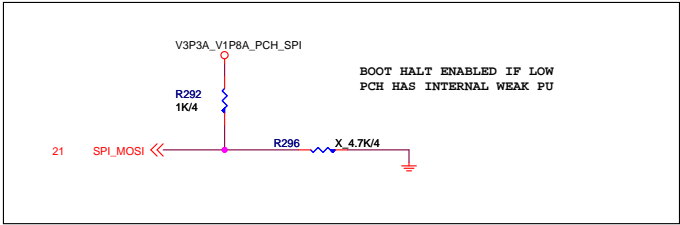
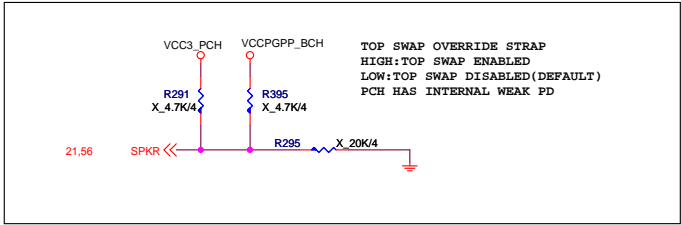


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GND



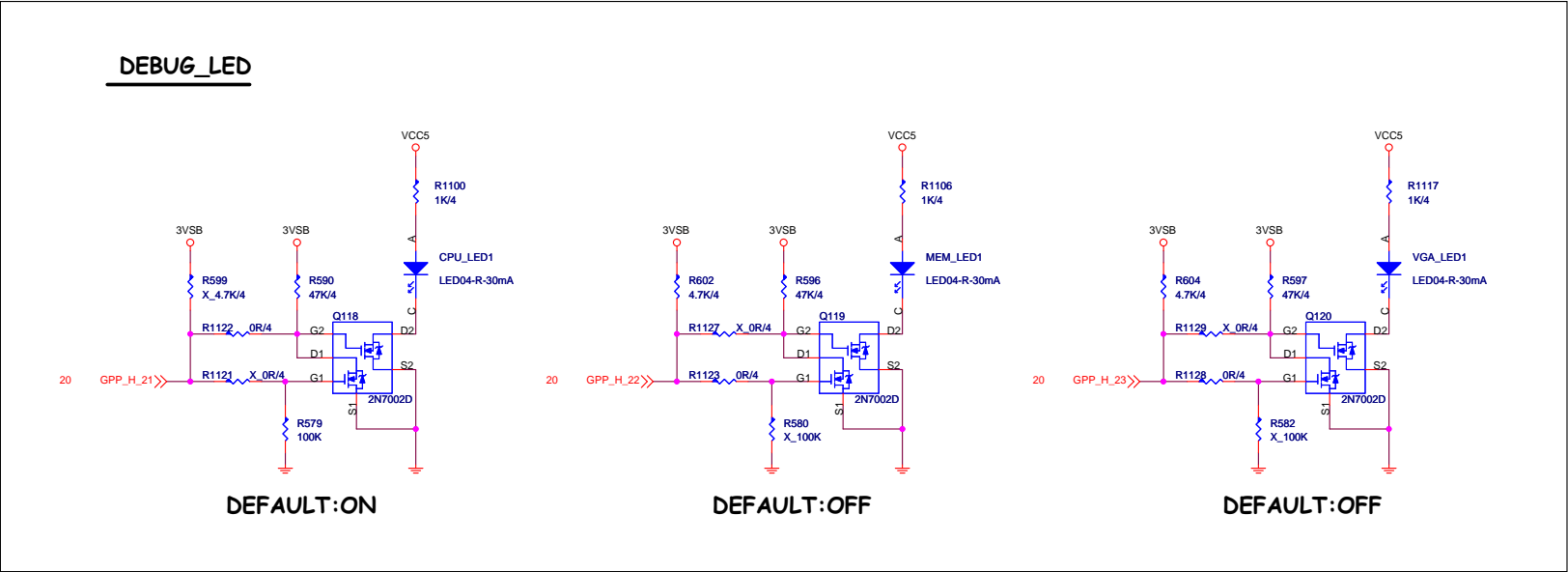
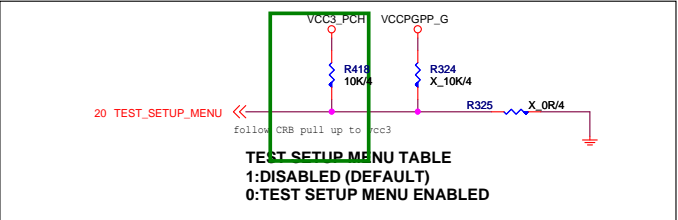
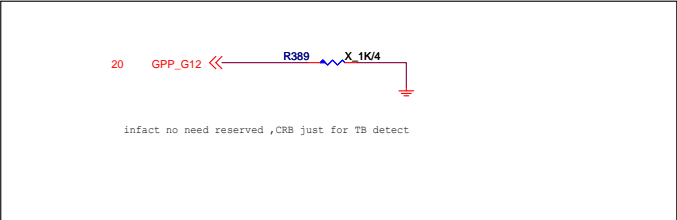
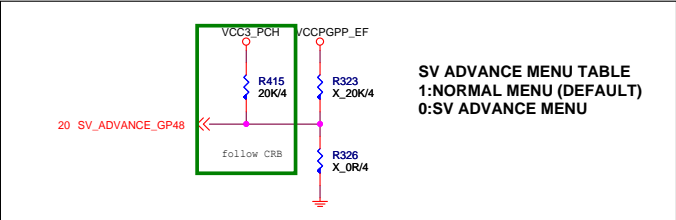
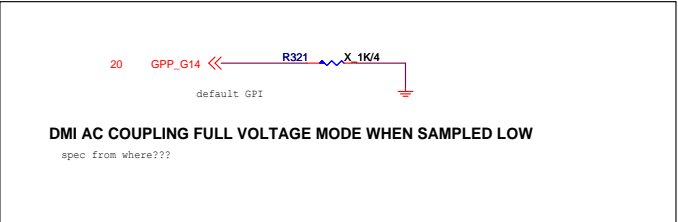
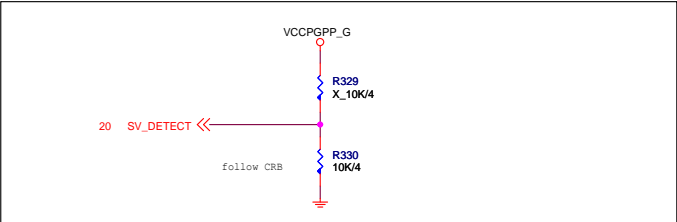
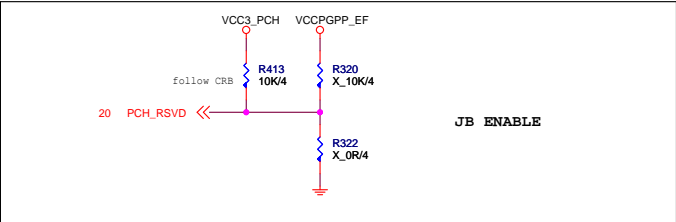
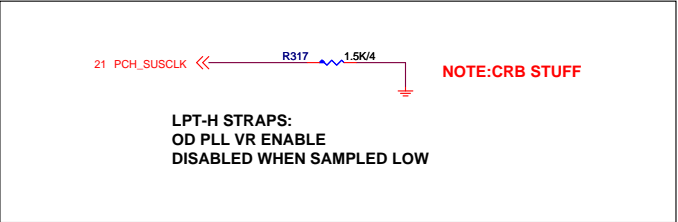
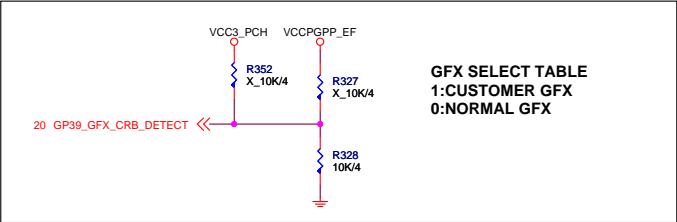
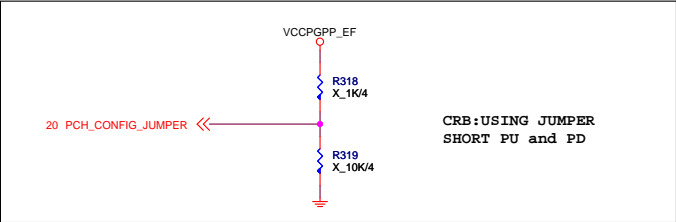
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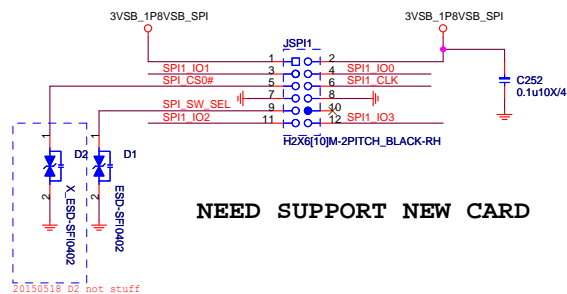
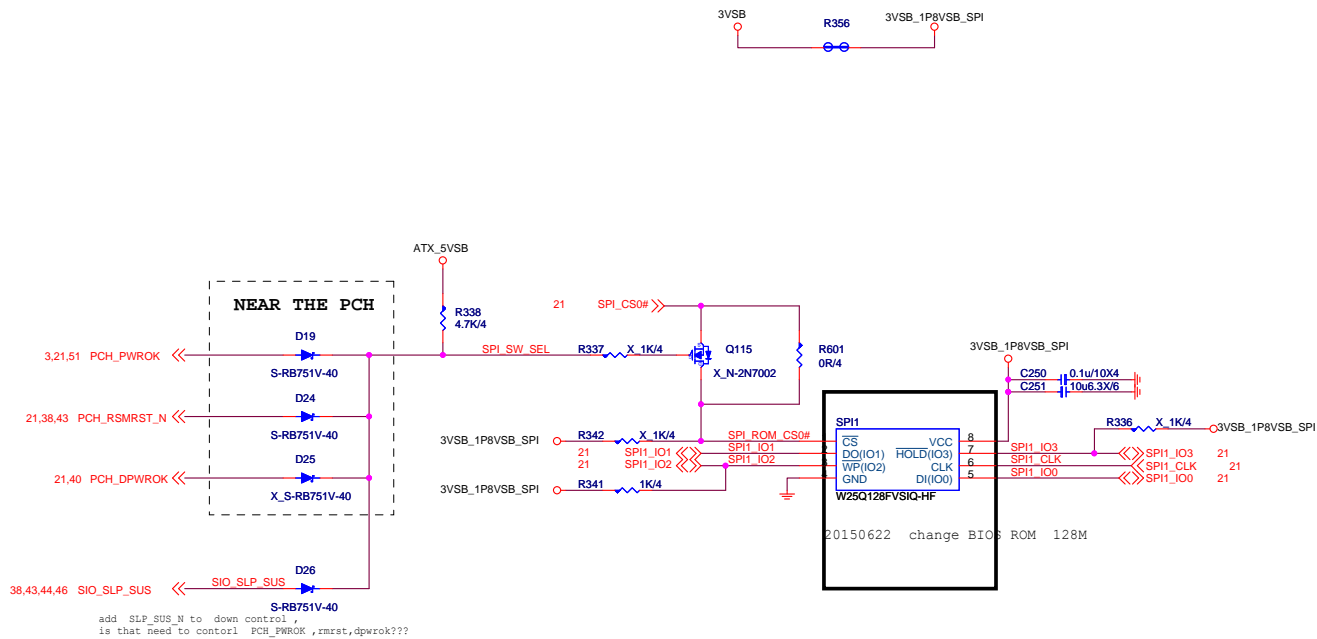
MICRO-STAR INT'L CO.,LTD

MS-7982

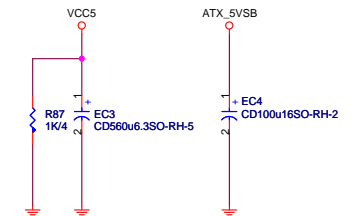
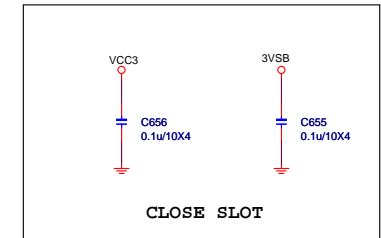
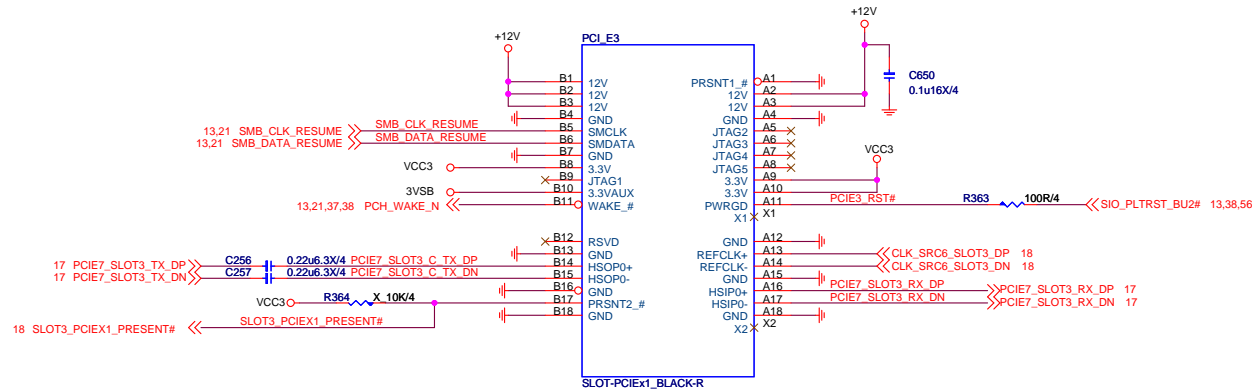
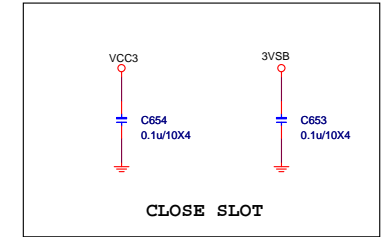
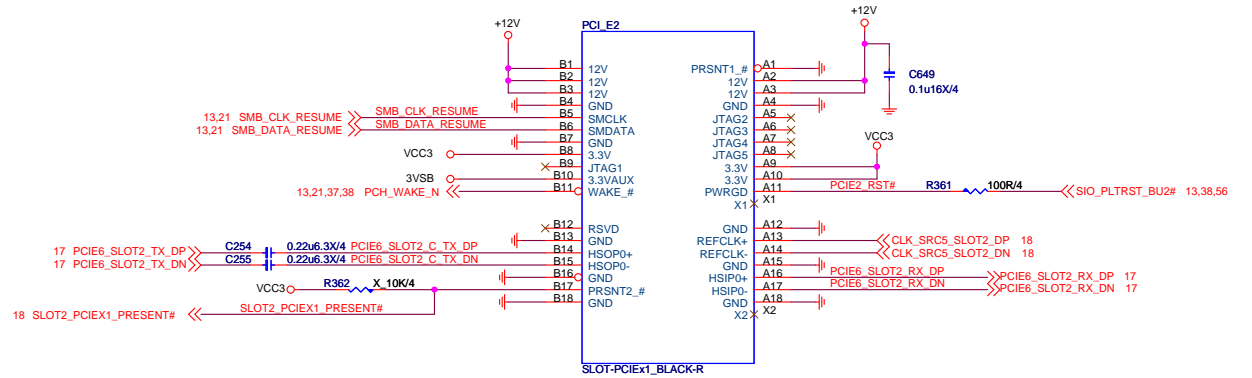
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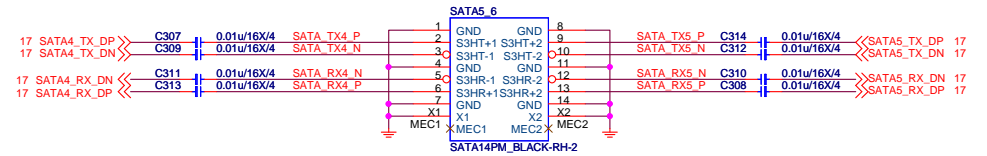
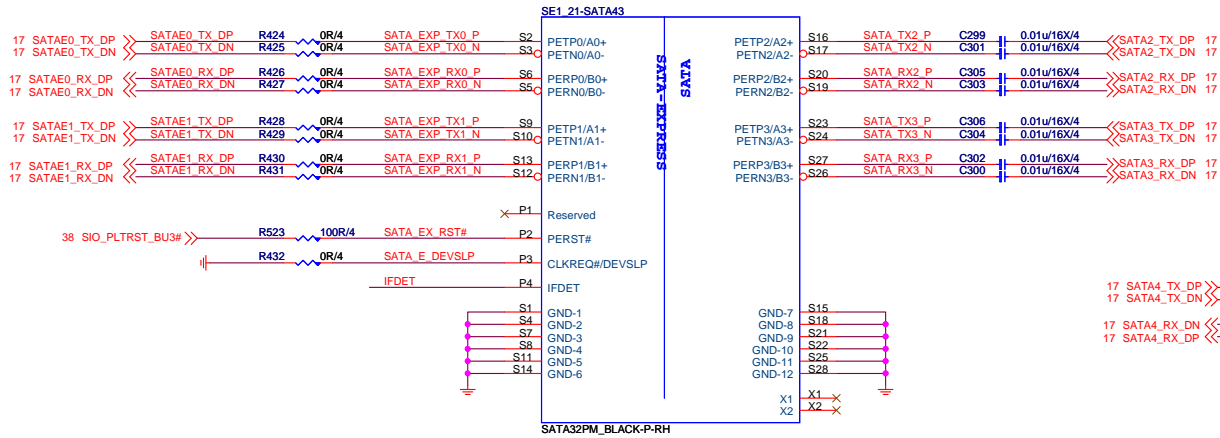
NEED SUPPORT NEW CARD

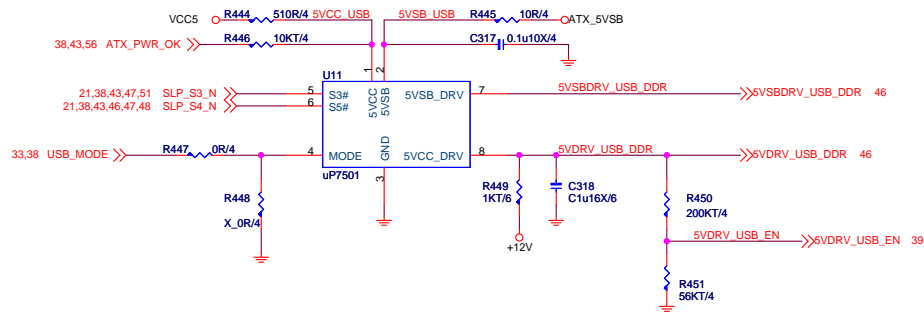


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

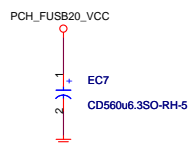
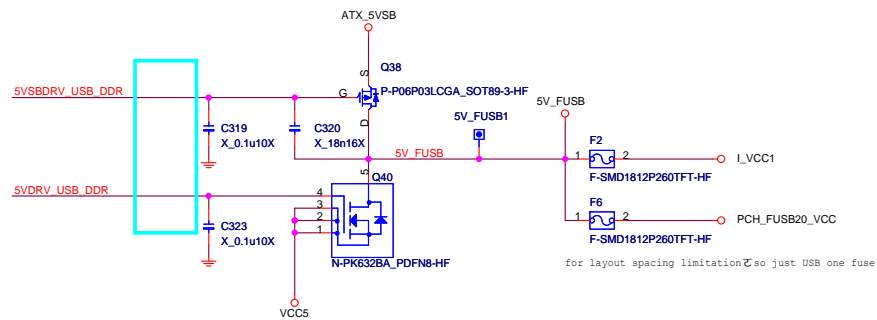


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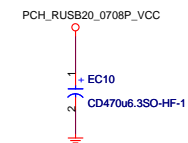
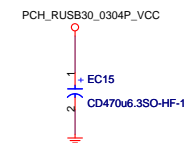
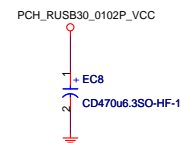
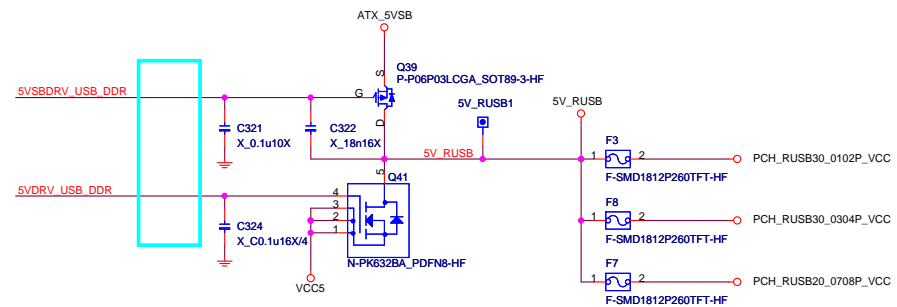




20150624 remove R452 R454 R453 R455



For 4 port usb,so keep 560uf

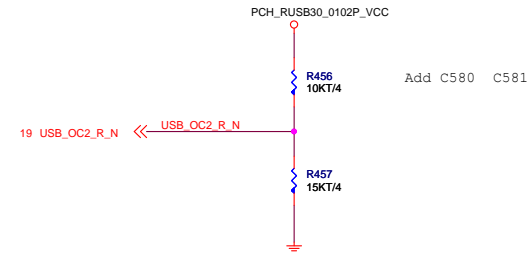
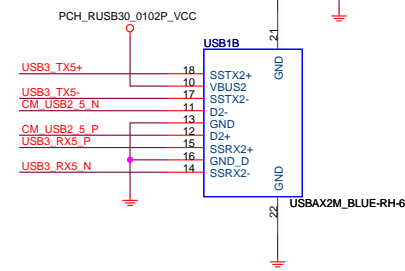
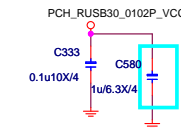
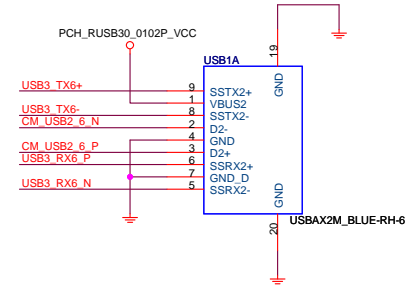
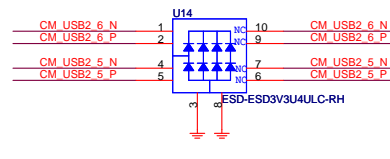
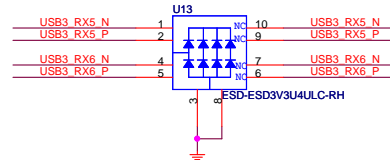
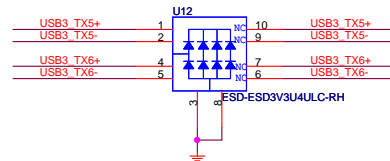
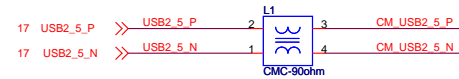
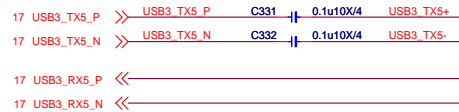


**MICRO-STAR INT'L CO.,LTD**

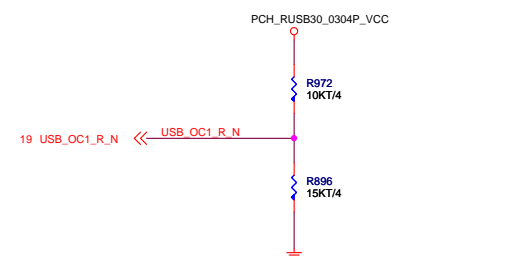
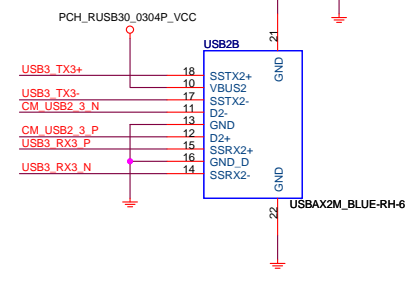
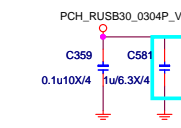
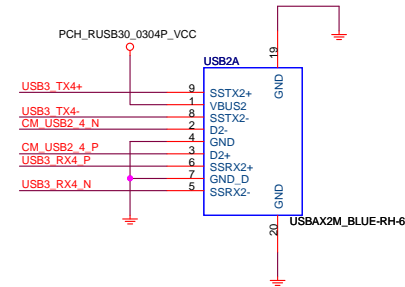
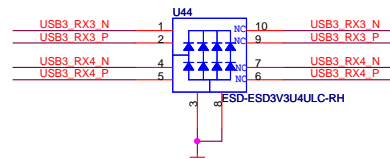
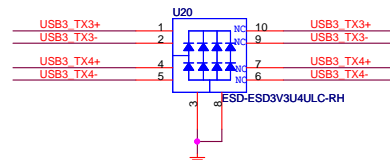
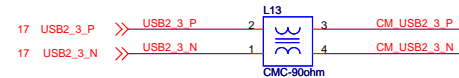
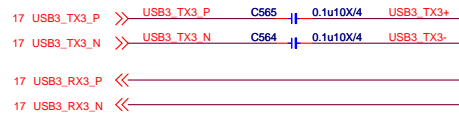
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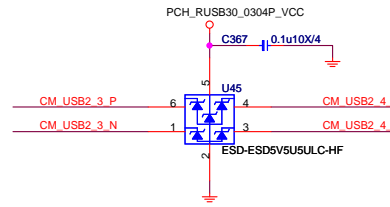
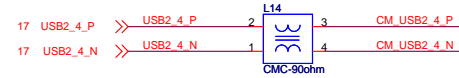
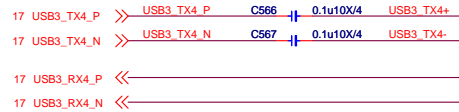
# USB3.0 PORT1



# USB3.0 PORT1



# USB3.0 PORT1

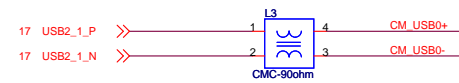
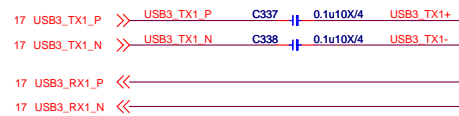


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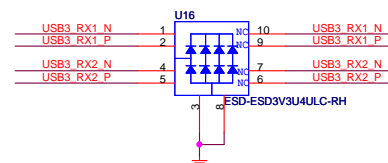
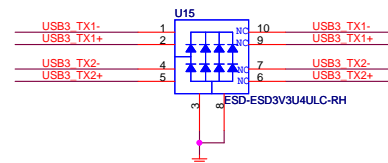
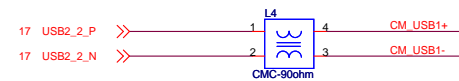
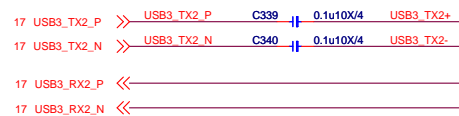


20150701 Remove USB3.0 Supper charge circuit,R377 R378 R375 R376 R382 R381 EC6 Remove

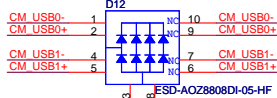
#### USB3.0 PORT1



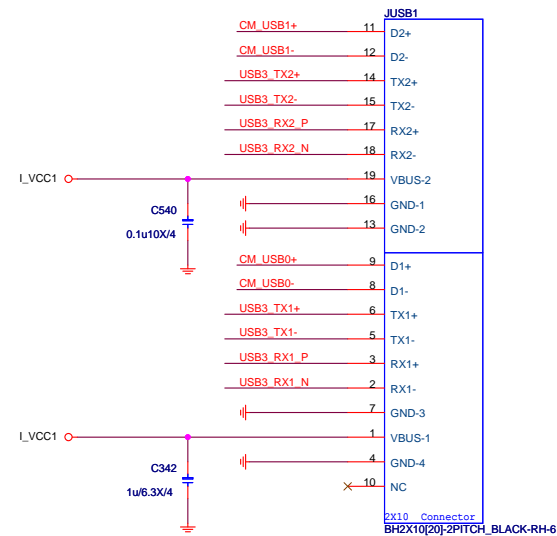
#### USB3.0 PORT1



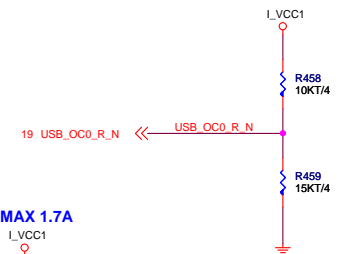
EMI suggestion.(default stuff)  
(use usb3.0 ESD for eye diagram)



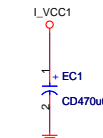
SLG55583A has internal ESD diode.



20150522 change list  
1. remove supper charge compent  
2. stuff R458 R459 R381  
3. stuff R377 R378 R375 R376



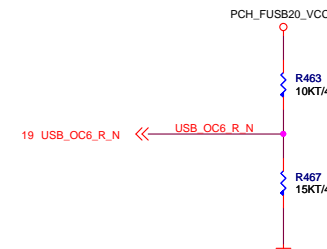
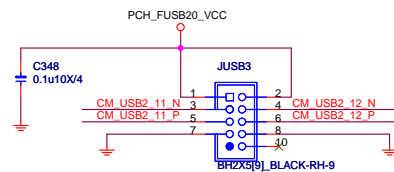
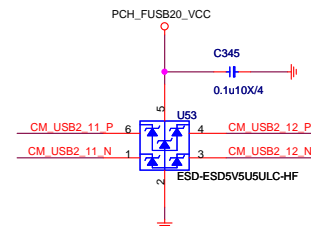
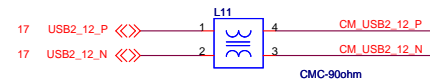
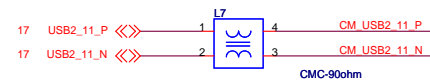
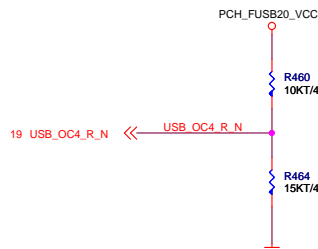
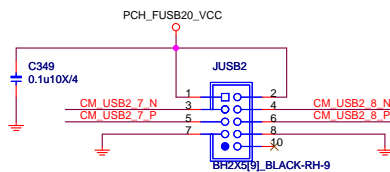
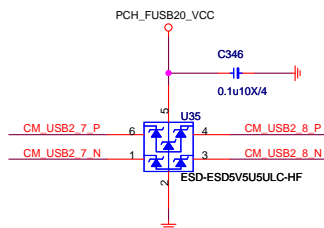
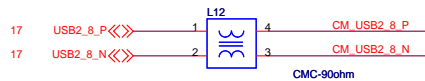
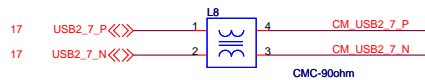
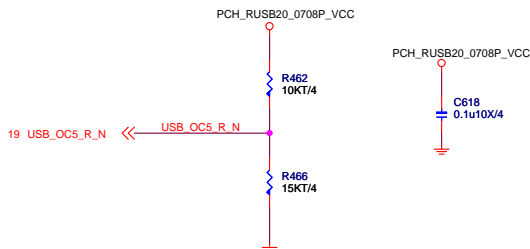
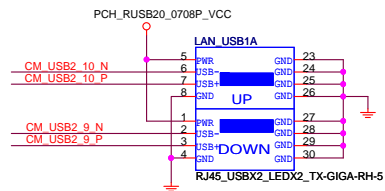
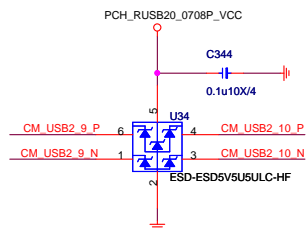
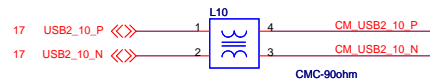
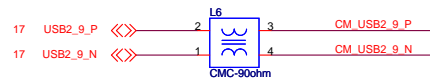
MAX 1.7A



MICRO-STAR INT'L CO.,LTD

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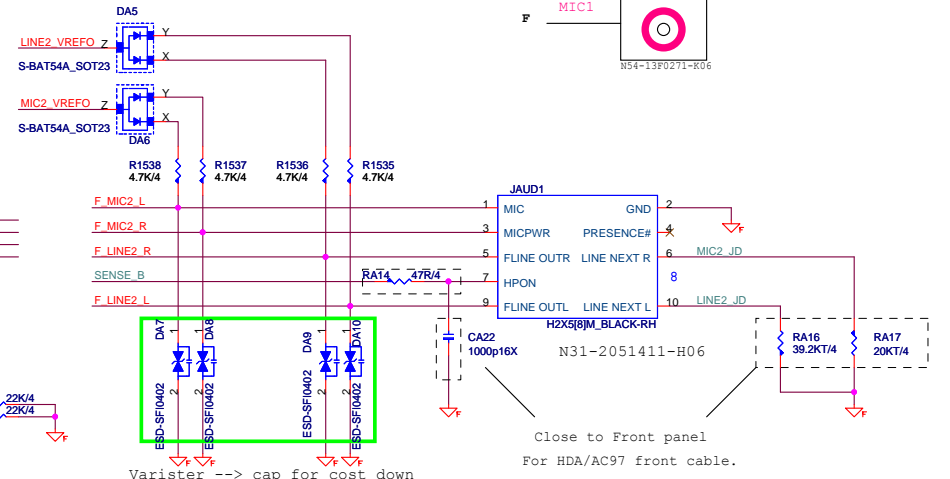
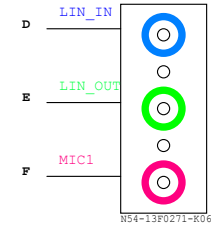
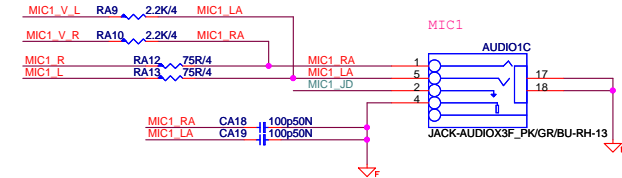
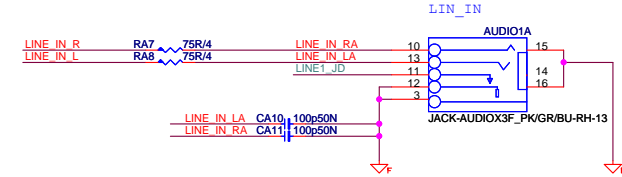
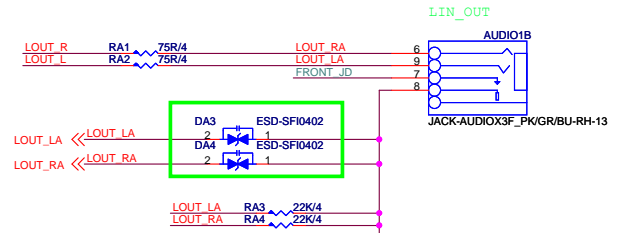
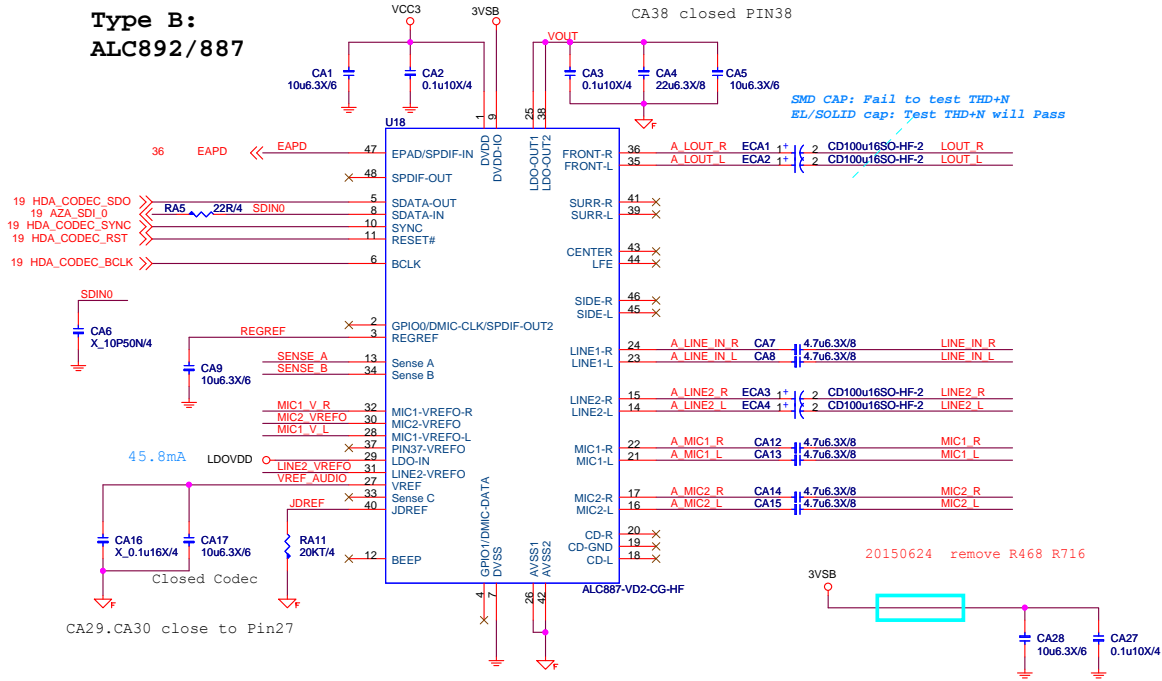
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# Type B: ALC892/887

CA4 closed PIN25  
CA3 closed PIN38  
CA38 closed PIN38

SMD CAP: Fail to test THD+N  
EL/SOLID cap: Test THD+N will Pass



Varister --> cap for cost down

D0G-2950500-SI0  
D0G-3010510-I05  
Close to Jack

Close to Front panel  
For HDA/AC97 front cable.



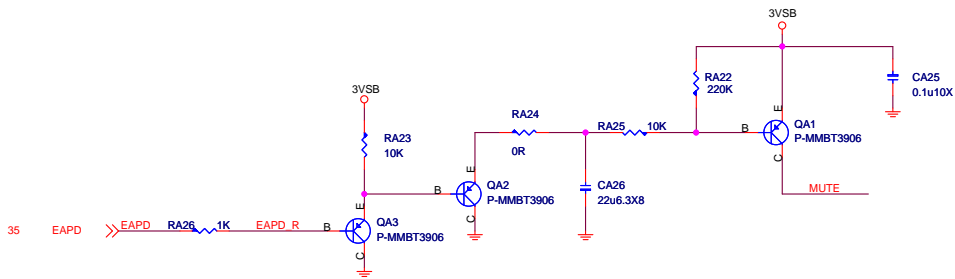
MICRO-STAR INT'L CO.,LTD

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## Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

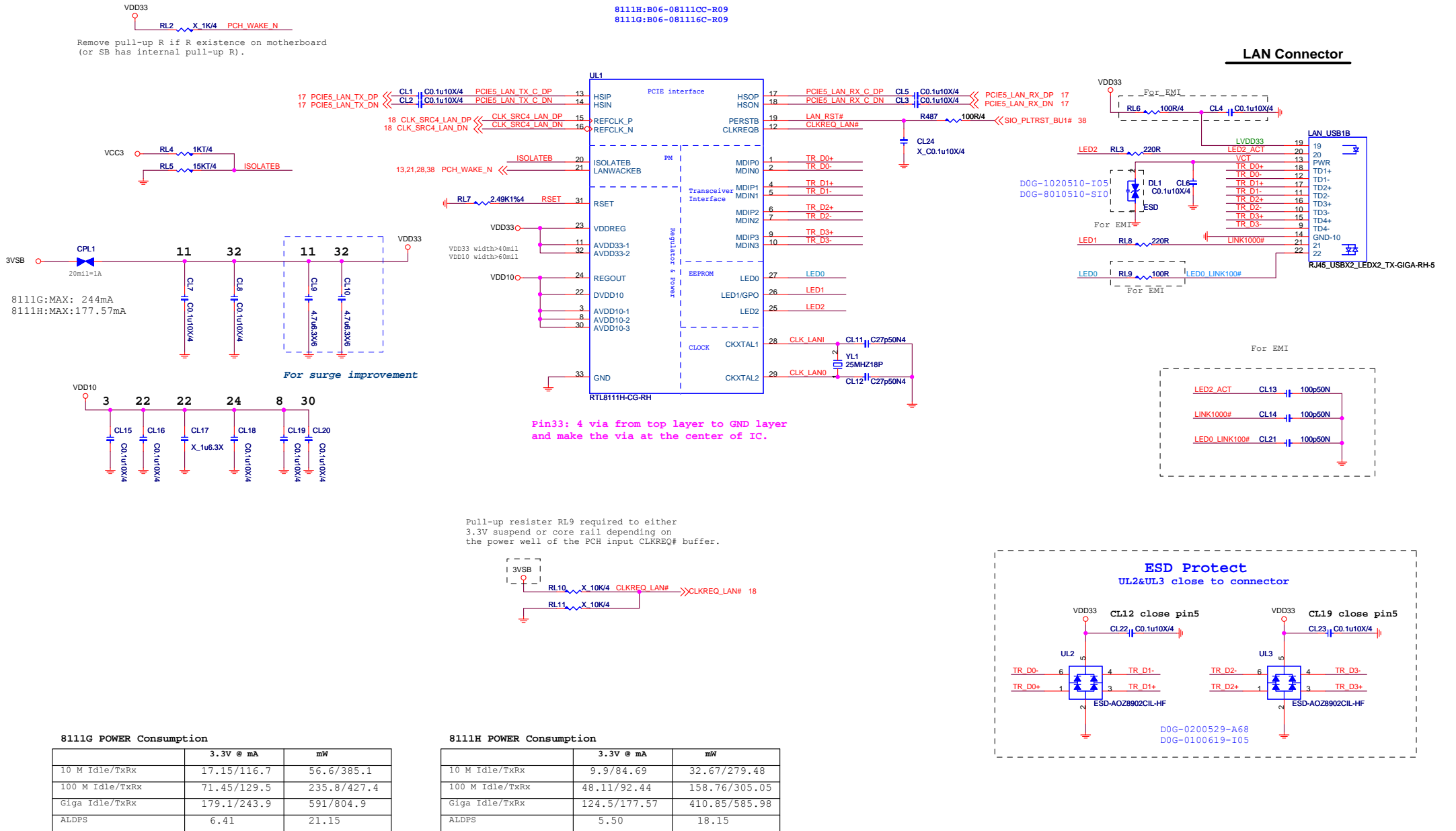
Analog



History:

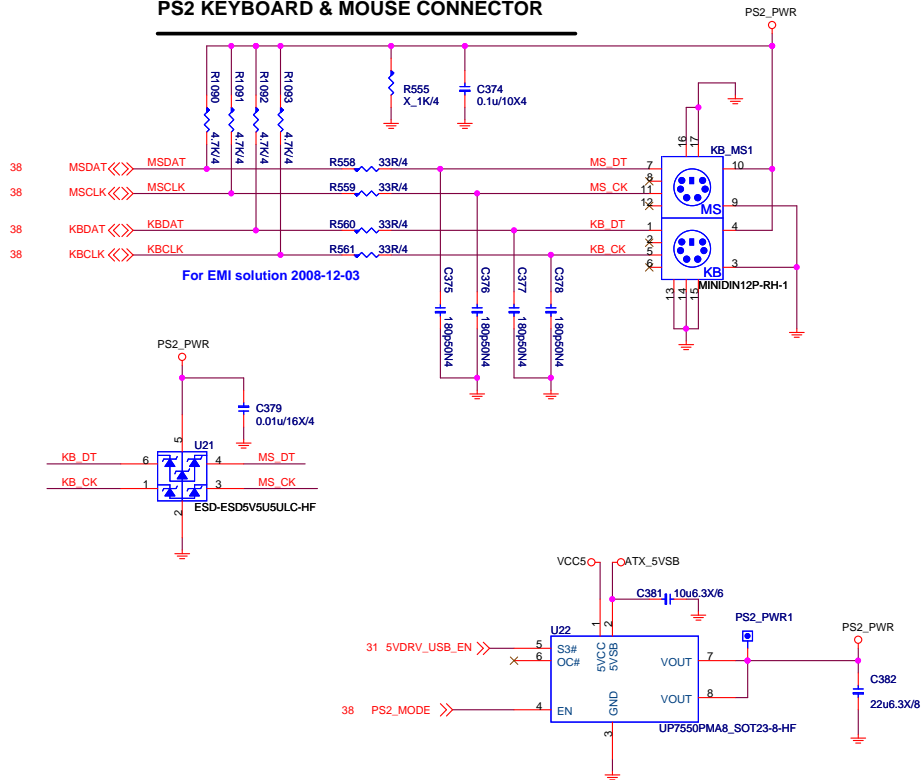
2014/02/13: stuff de-pop circuit of Line out & HP out.

# RTL8111G/RTL8111H Giga LAN

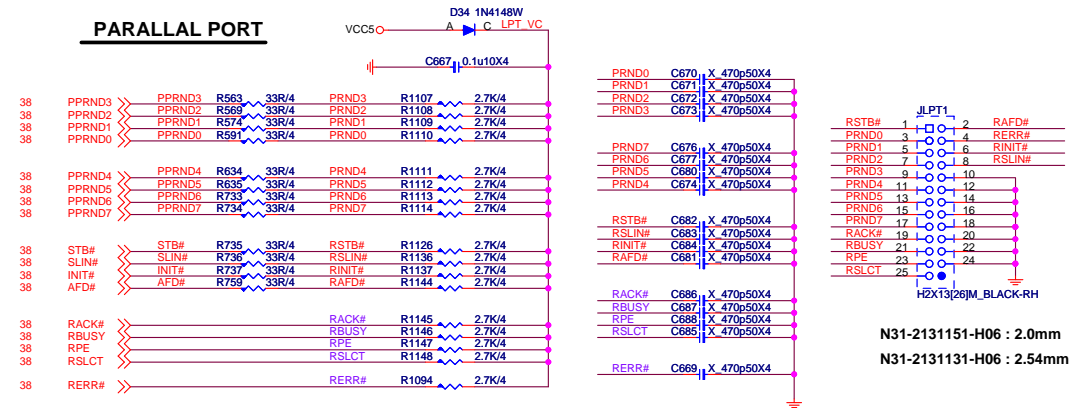




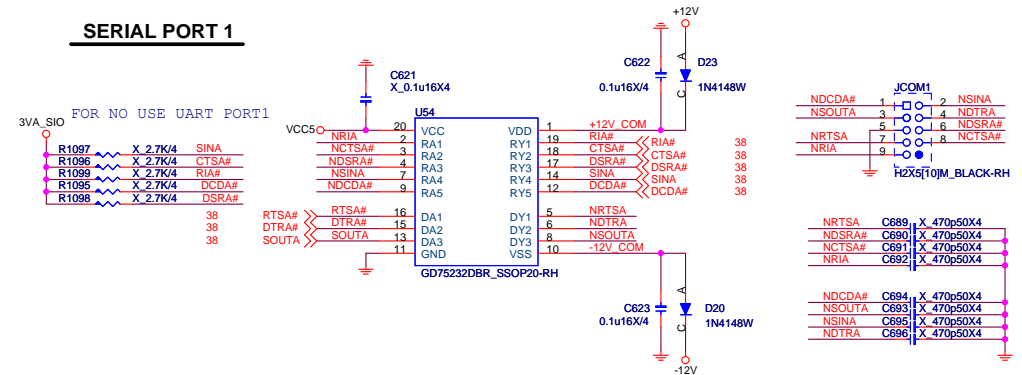
## PS2 KEYBOARD & MOUSE CONNECTOR



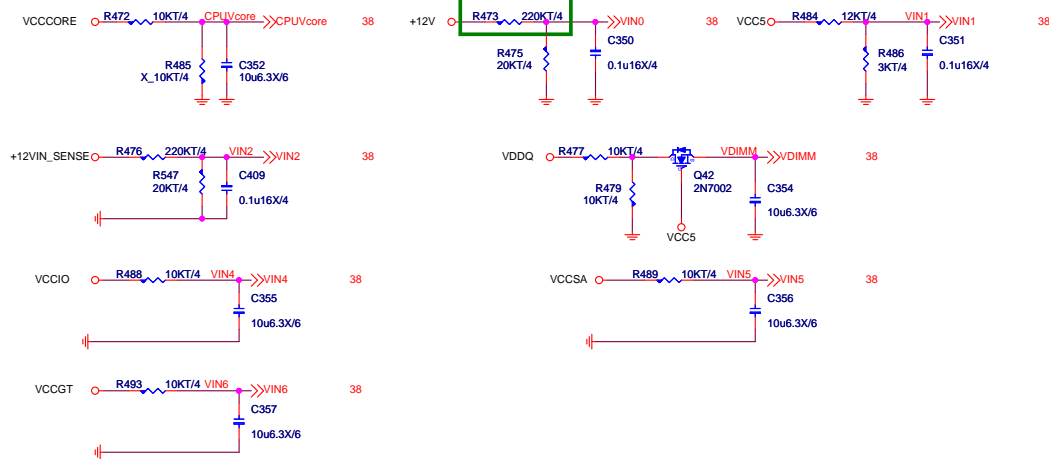
## PARALLAL PORT

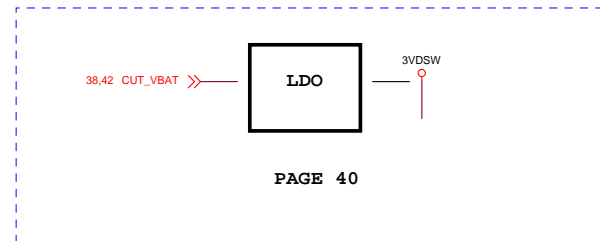
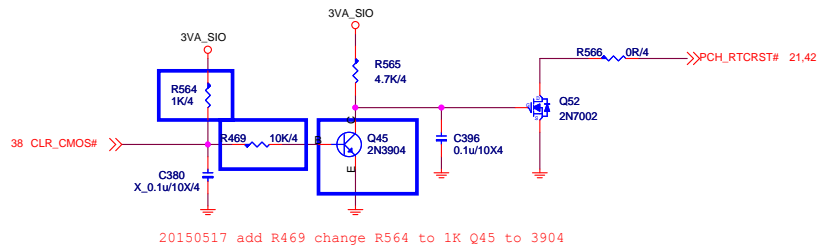
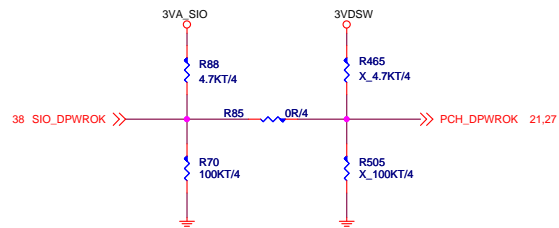
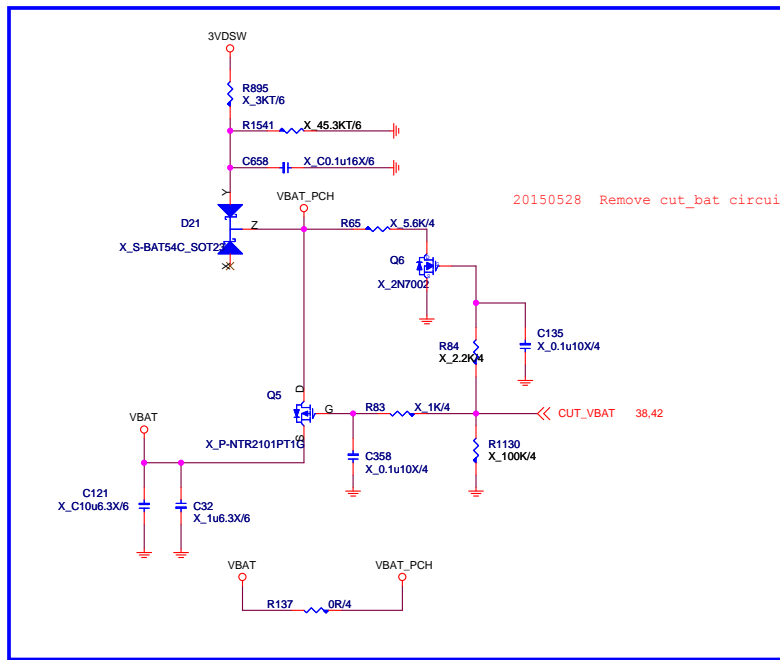


## SERIAL PORT 1

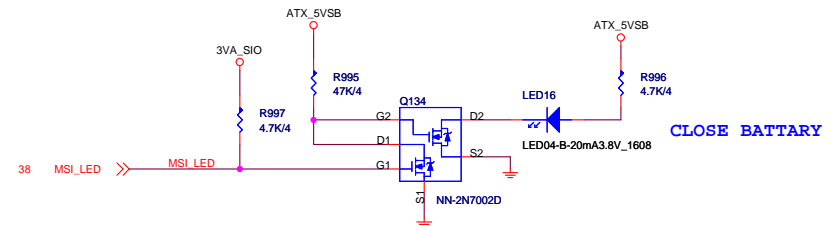
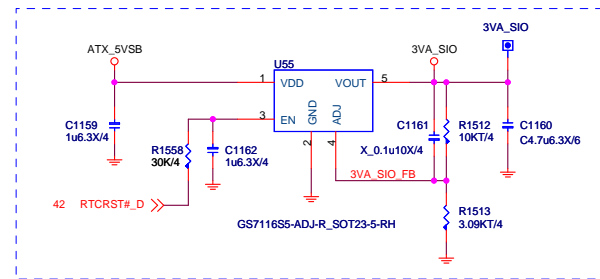
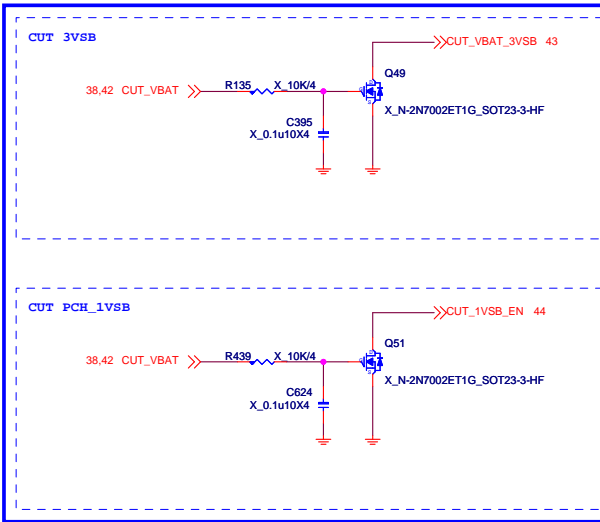


## HW Monitor - Voltage



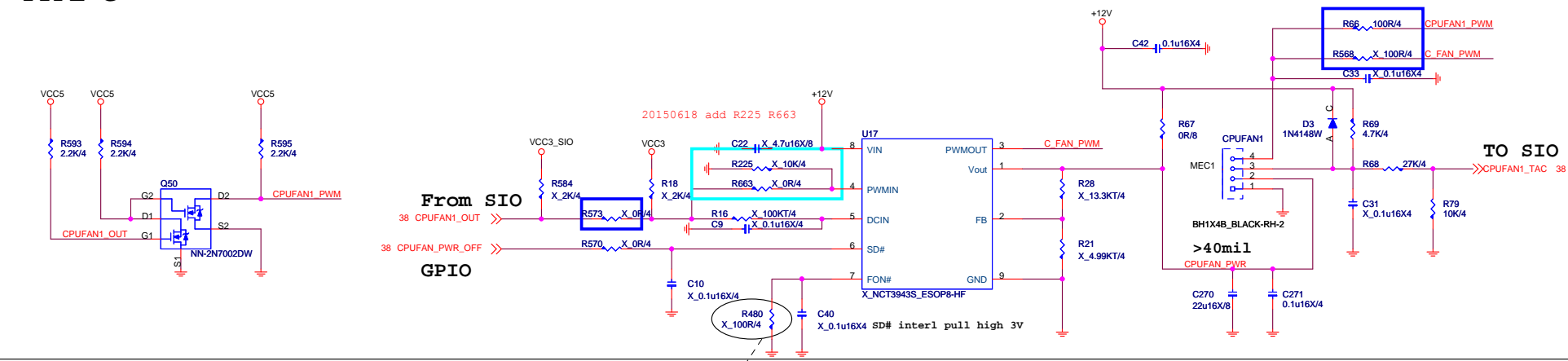


20150528 Remove cut\_bat circuit

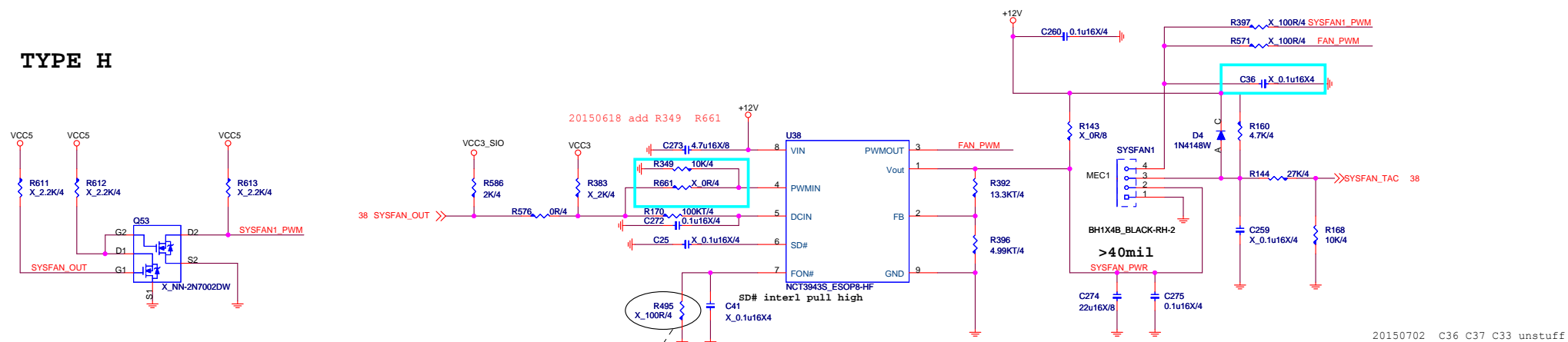




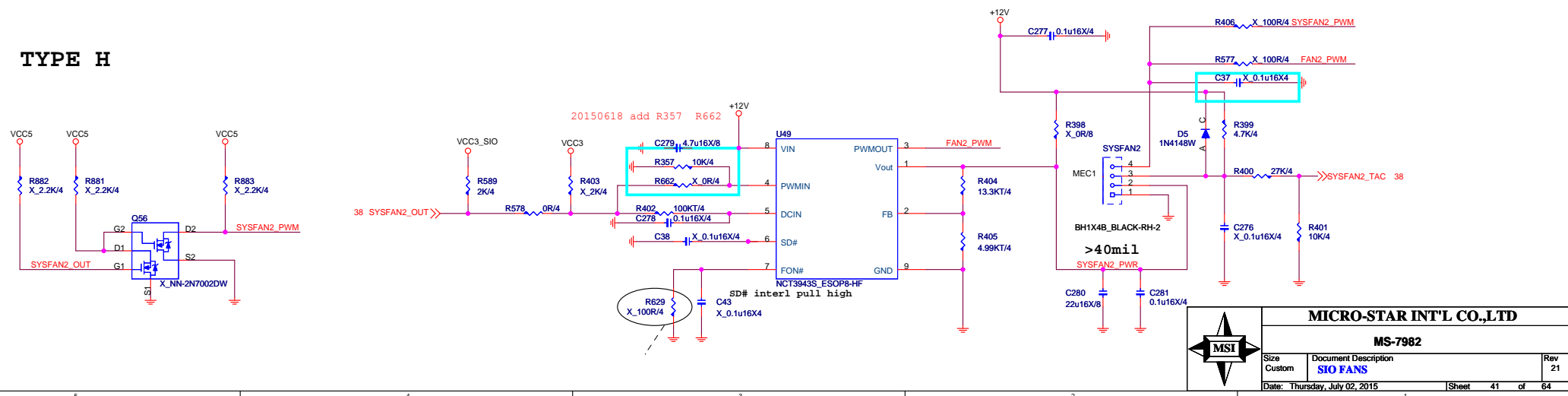
**TYPE G**



**TYPE H**

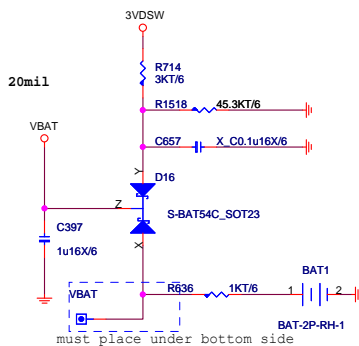


**TYPE H**

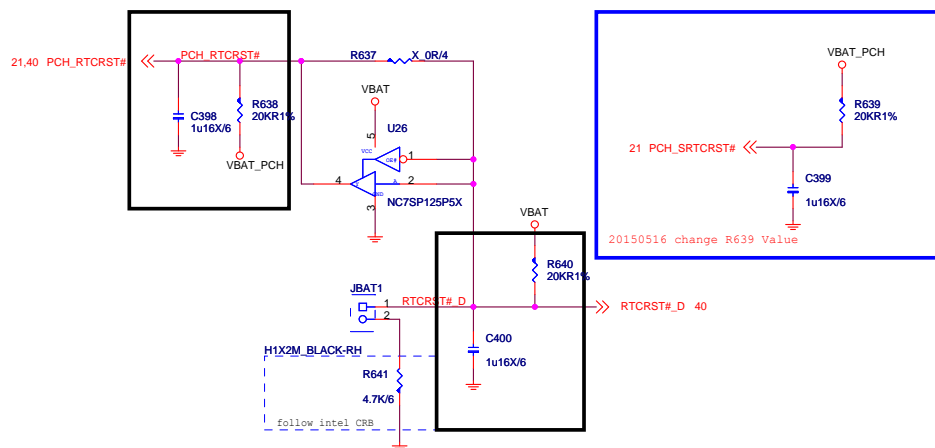


## G3 Status

NOTE: CAN'T EXCEED 3.2V



tPCH01:(VccRTC\_90% -> RTCRST#\_High) > 9mS



tPCH04:(VccRTC\_90% -> DSW\_Start) > 9mS  
(USED FOR NO BATTERY)



tPCH05:(RTCRST#\_High -> DSW\_PWROK\_High) > 1uS  
(USED FOR NO BATTERY)



BATLOW\_N

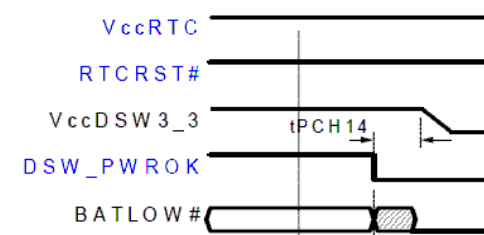
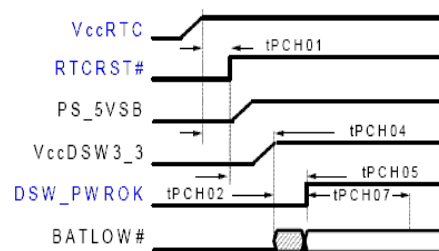
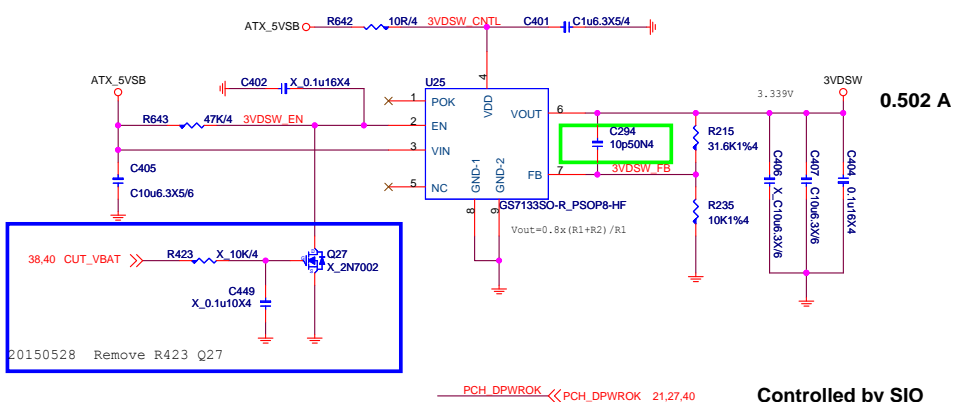
BATLOW\_N

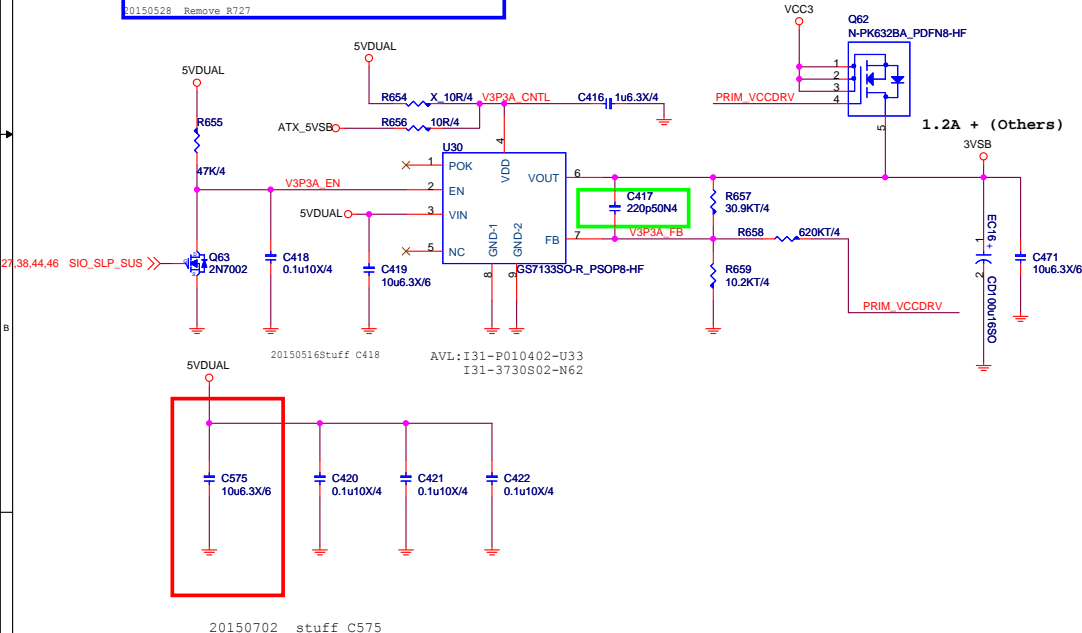
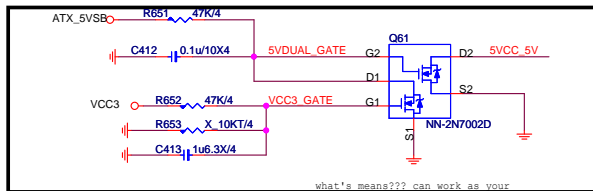
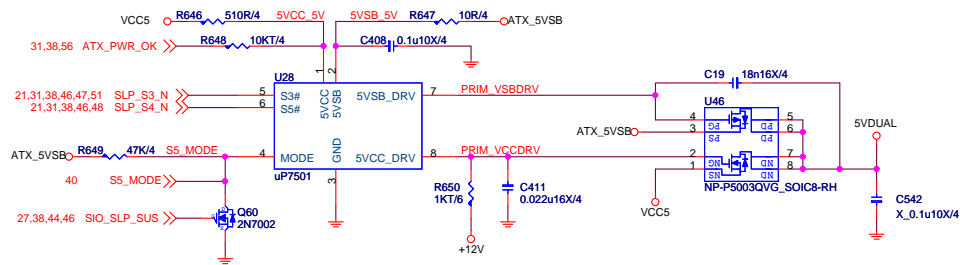
21

PCH will sample BATLOW# on the rising edge of DSW\_PWROK for DSx Systems

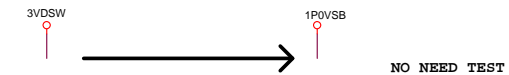
## DEEP S4/S5 Status

tPCH02:(VccDSW\_90% -> DSW\_PWROK\_High) > 10mS

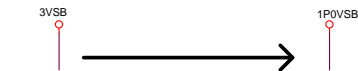




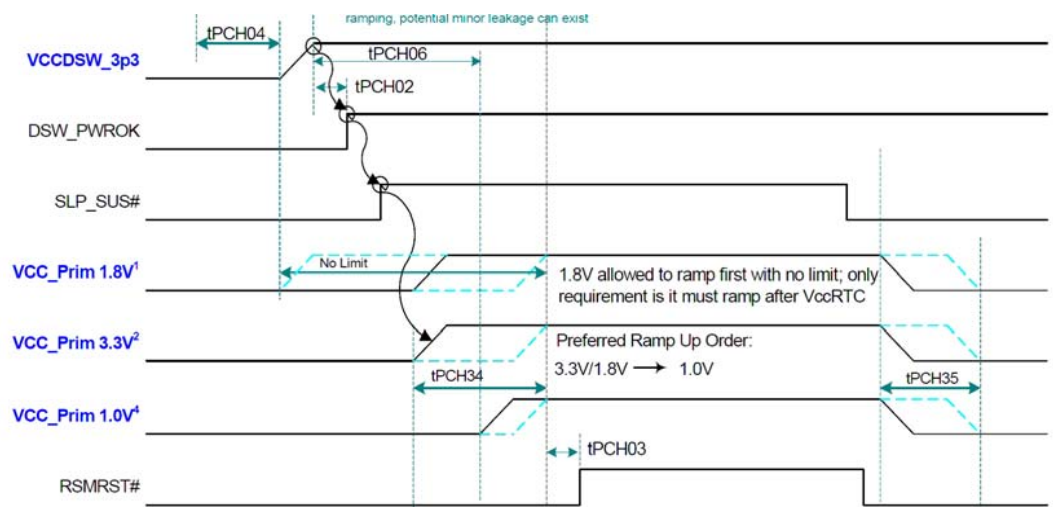
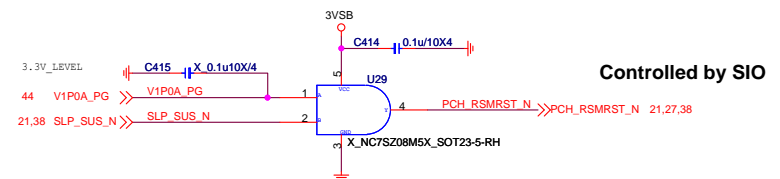
tPCH06:(VccDSW\_95% -> VccPrim\_1.0\_Start) > 200uS



tPCH34:0 < (All PCH Primary Rails should ramp up within this window) < 20mS  
tPCH35:0 < (All PCH Rails should ramp down within this window) < 100mS



tPCH03:(VccPrim\_1.0\_95% -> RSMRST#\_High) > 10mS



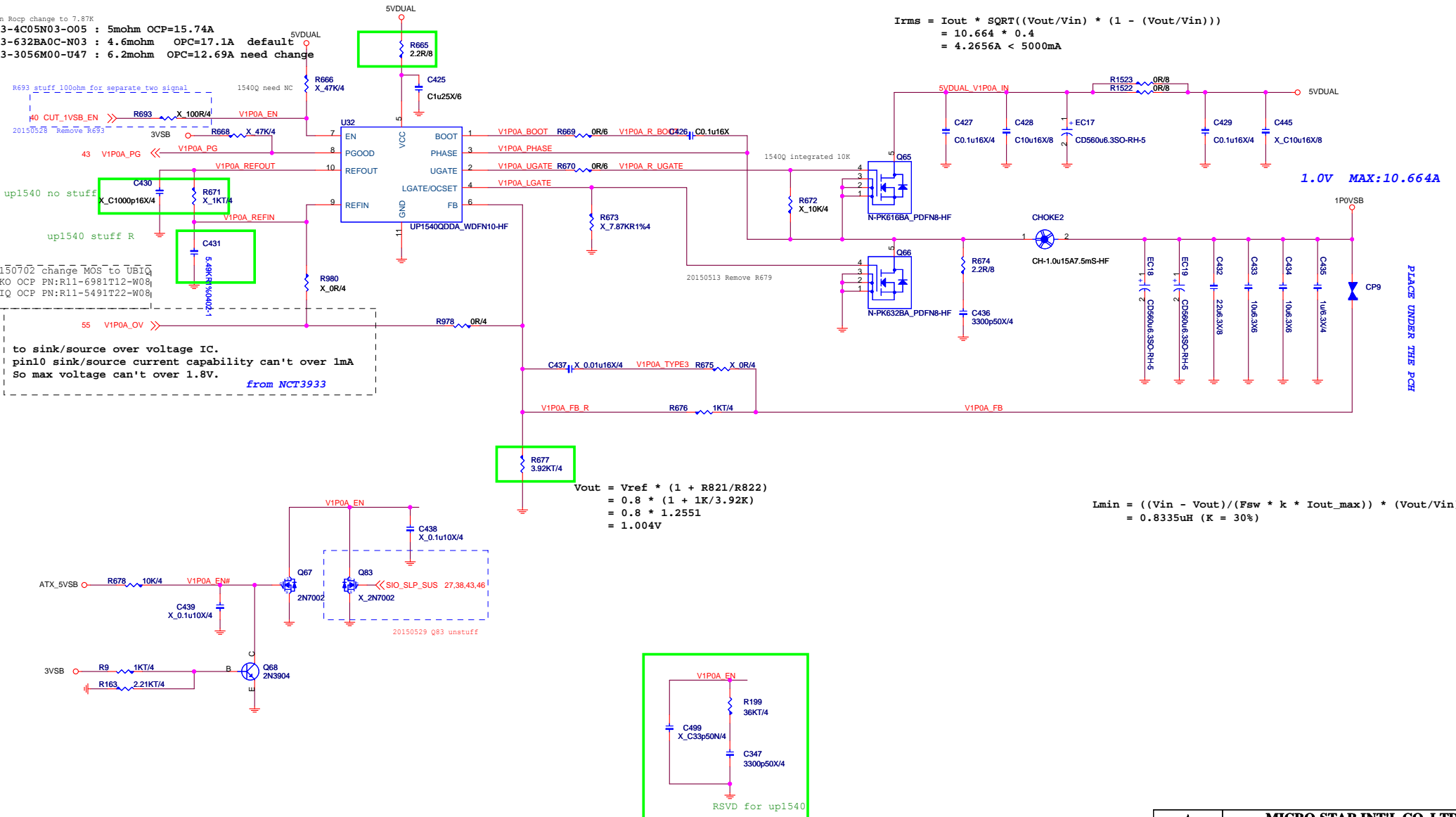
Rdson(low) 4.5V  
D03-4C05N03-O05 : 5mohm  
D03-632BA0C-N03 : 4.6mohm  
D03-3056M00-U47 : 6.2mohm  
D03-3116M00-U47 : 3.6mohm

1.0V MAX:10.664A  
OCP :10A\*1.5=15A

Rocset = 1.5 \* Imax \* Rdson(low) / Iocset  
= 1.5 \* 10 \* 3.6mohm / 10uA  
=5.4K

when Rocp change to 7.87K

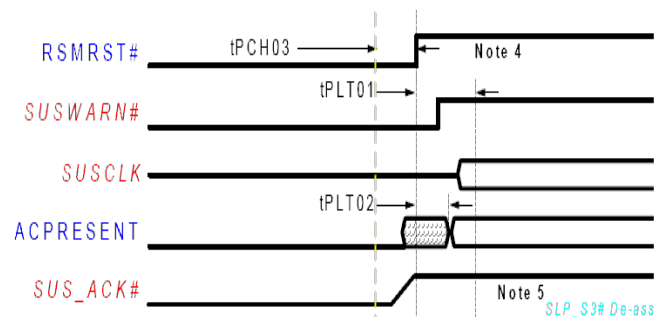
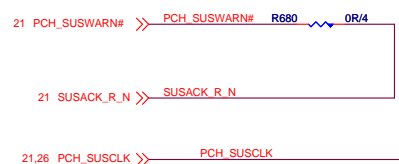
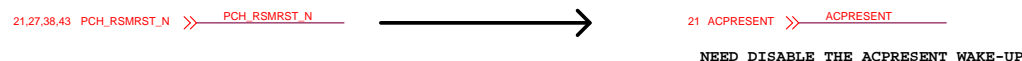
D03-4C05N03-O05 : 5mohm OCP=15.74A  
D03-632BA0C-N03 : 4.6mohm OPC=17.1A default  
D03-3056M00-U47 : 6.2mohm OPC=12.69A need change



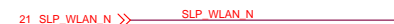
tPLT01:(RSMRST#\_High -> SUSPWRDNACK\_Valid) > 200mS  
(Just Used For Non-Deep Sx PLF, This is no-used)



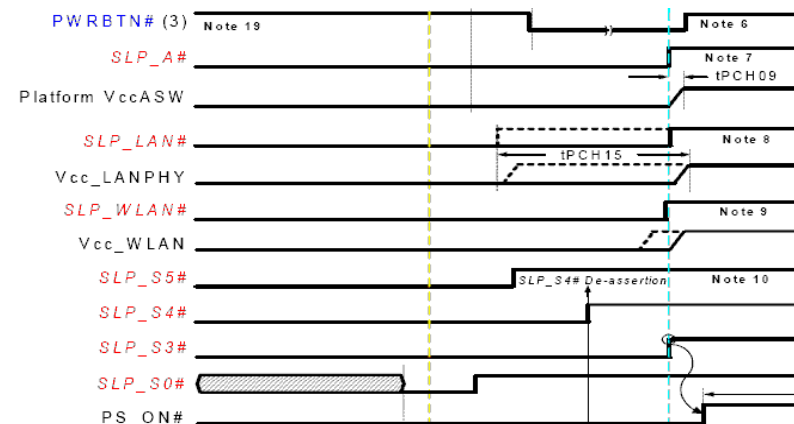
tPLT02:(RSMRST#\_High -> ACPRESENT\_Valid) < 0mS



The PCH no longer have a dedicated ASW rail



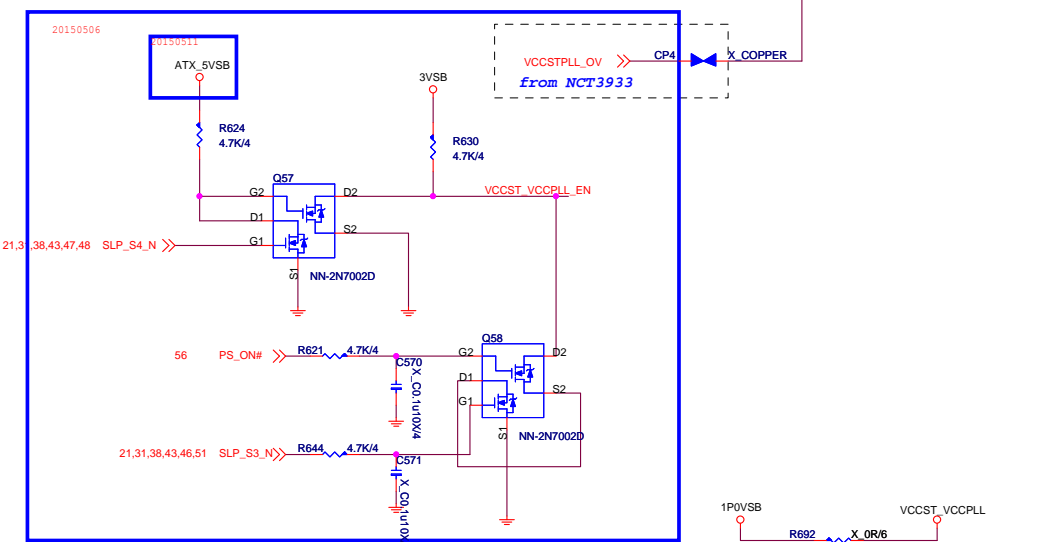
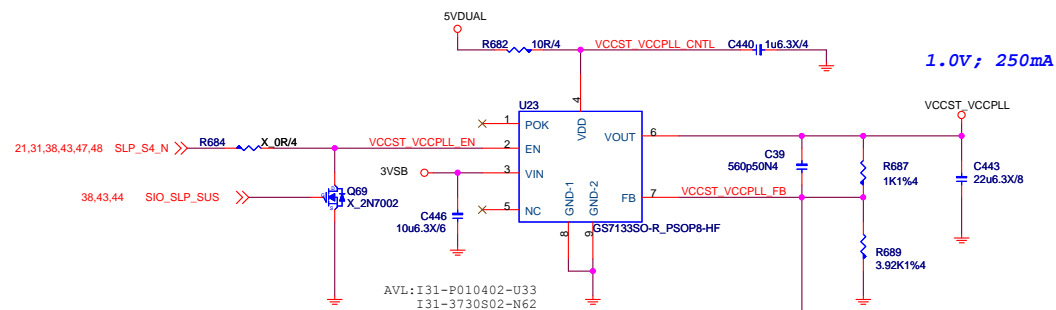
S0 Sleep Control. When PCH is idle and processor is in C10 state, this pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.



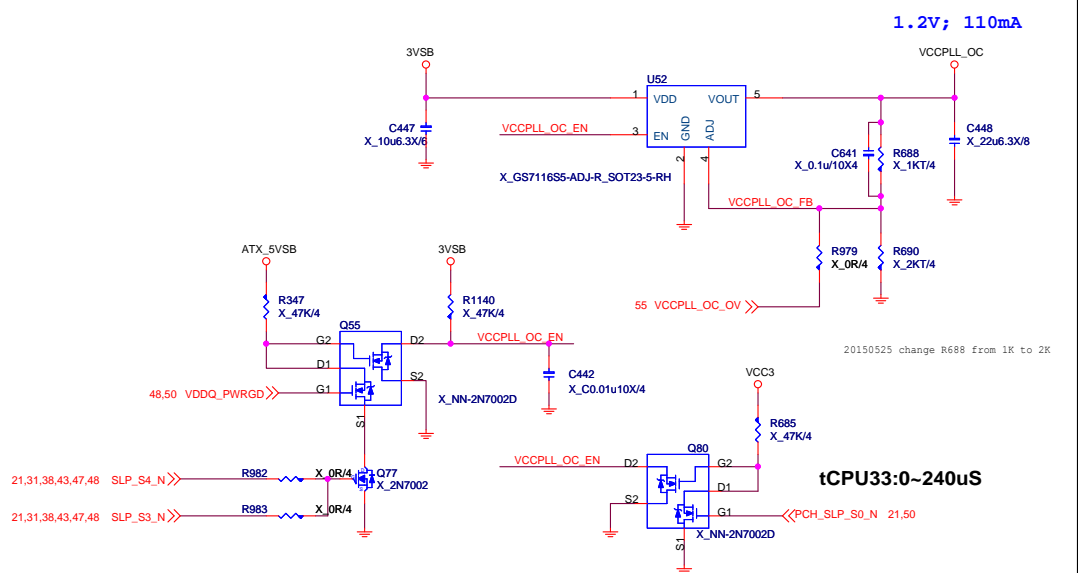
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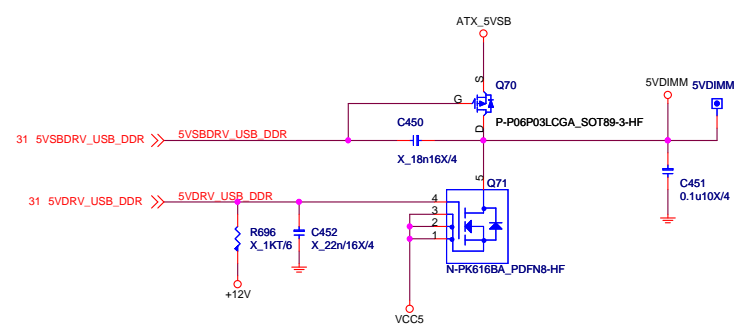
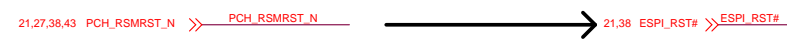
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VCCST and VCCPLL can remain powered during S4 and S5 pwr states for board VR optimization. VCCST may also remain powered in S4 and S5 for debug purposes. Refer to debug port design guide for more details.



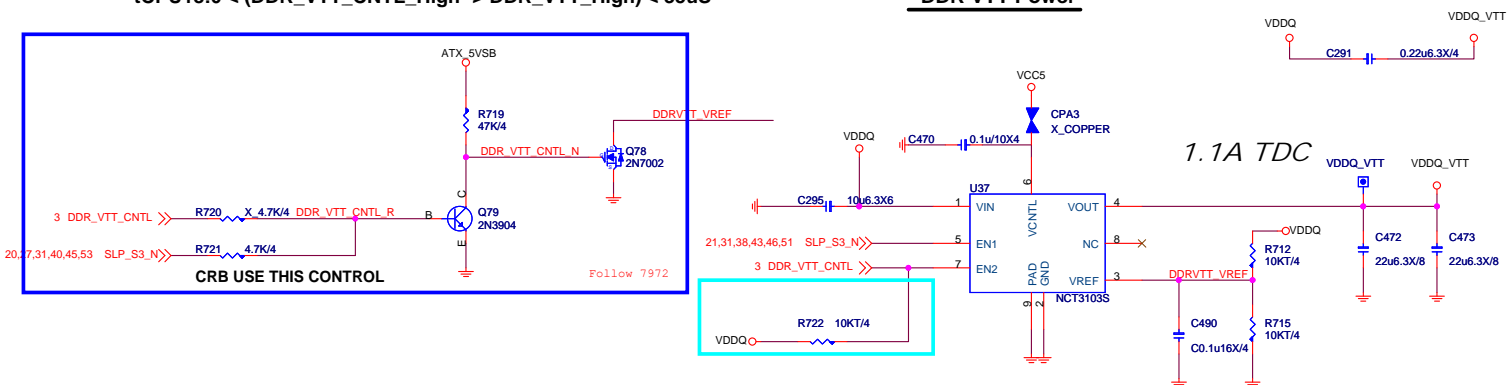
tPCH18:(RSMRST#\_High -> ESPI\_RESET#\_High) > 90uS



To make sure VPP EN after 5VDIMM stable

tCPU18:0 < (DDR\_VTT\_CNTL\_High -> DDR\_VTT\_High) < 35uS

### DDR VTT Power



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DDR4\_1.2V 2.5A+9.5A+1.2A=13.2A  
2.5A FOR CPU  
9.5A FOR 4DIMM  
1.2A FOR DDR VTT

OCp :13.2A\*1.5=19.8A

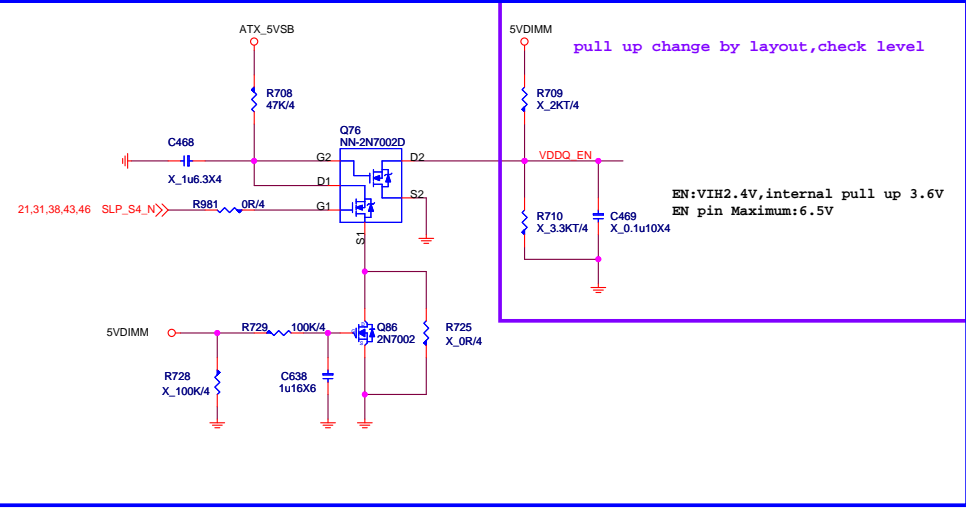
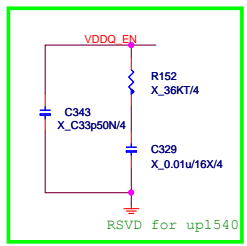
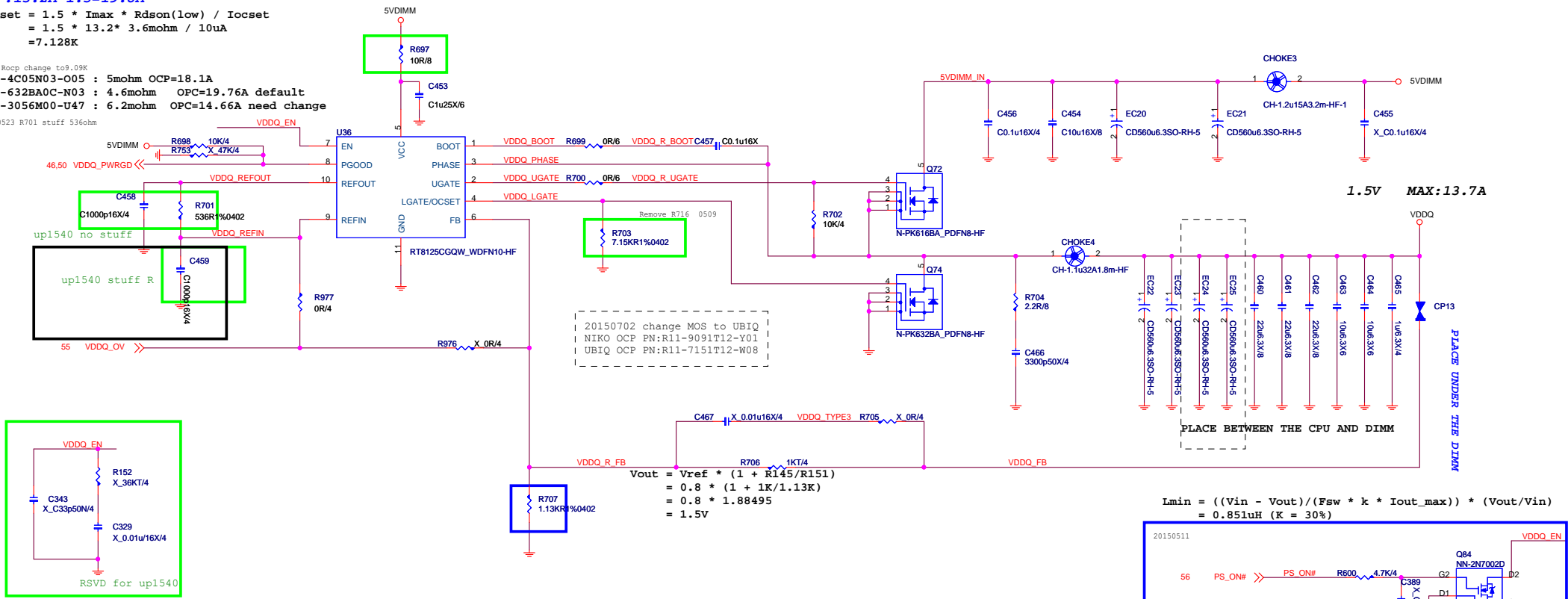
Rocset = 1.5 \* I<sub>max</sub> \* R<sub>ds(on)</sub>(low) / I<sub>ocset</sub>  
= 1.5 \* 13.2 \* 3.6mohm / 10uA  
=7.128K

when Rocp change to9.09K  
D03-4C05N03-O05 : 5mohm OCP=18.1A  
D03-632BA0C-N03 : 4.6mohm OPC=19.76A default  
D03-3056M00-U47 : 6.2mohm OPC=14.66A need change  
20150523 R701 stuff 536ohm

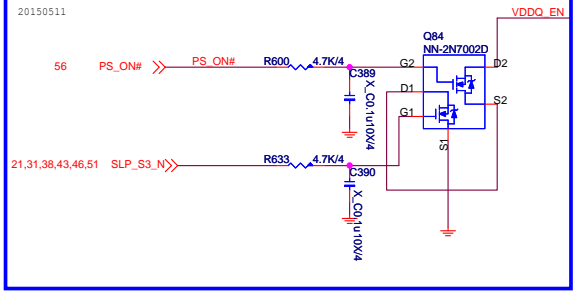
2015.01.22  
for up1540:R189->2.2R,C187->1uF  
for RT8125:R189->10R,C187->1uF

R <sub>ds(on)</sub> (low)	4.5V
D03-4C05N03-O05	: 5mohm
D03-632BA0C-N03	: 4.6mohm
D03-3056M00-U47	: 6.2mohm
D03-3116M00-U47	: 3.6mohm

I<sub>rms</sub> = I<sub>out</sub> \* SQRT((V<sub>out</sub>/V<sub>in</sub>) \* (1 - (V<sub>out</sub>/V<sub>in</sub>)))  
= 15 \* 0.4582  
= 6.87A < (4700\*2)mA



L<sub>min</sub> = ((V<sub>in</sub> - V<sub>out</sub>)/(F<sub>sw</sub> \* k \* I<sub>out\_max</sub>)) \* (V<sub>out</sub>/V<sub>in</sub>)  
= 0.851uH (K = 30%)

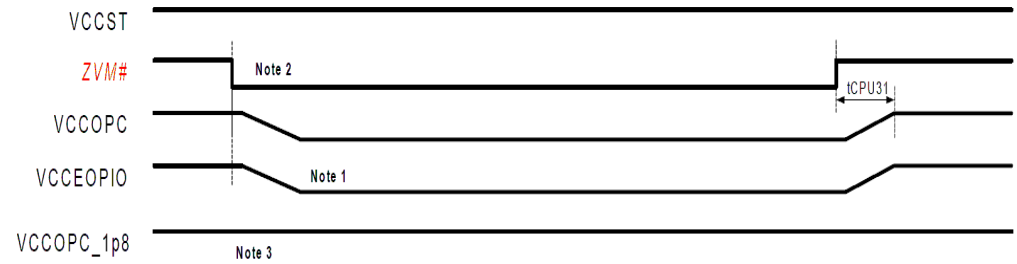
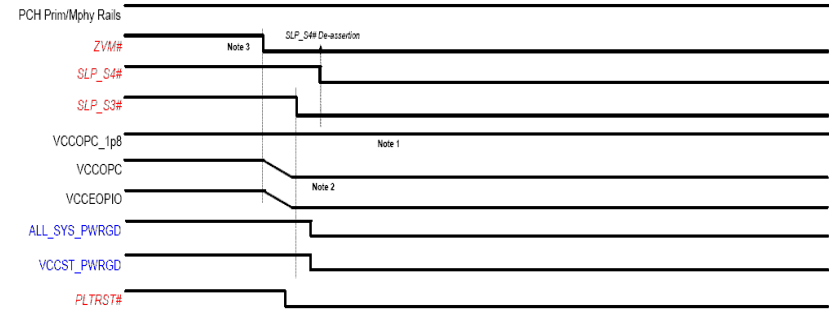
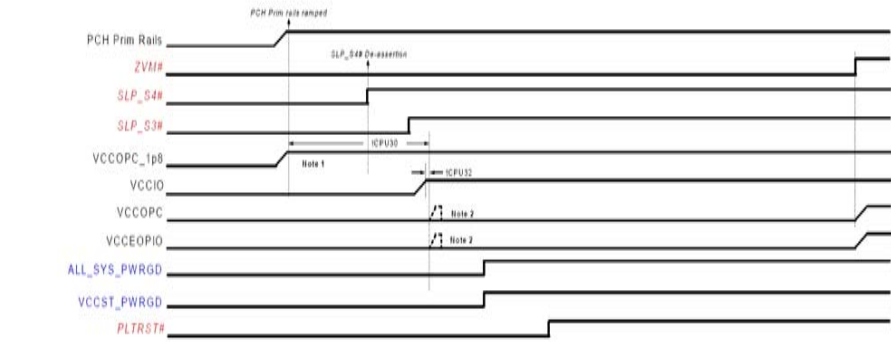




JUST ON Processors w/ on  
package cache

3,51,54 VR\_READY >>  
21,38,56 PLTRST\_N >> RESERVE

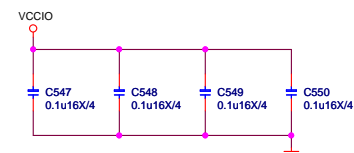
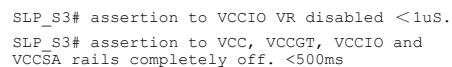
3,51,54 VR\_READY >>  
21,38,56 PLTRST\_N >> RESERVE

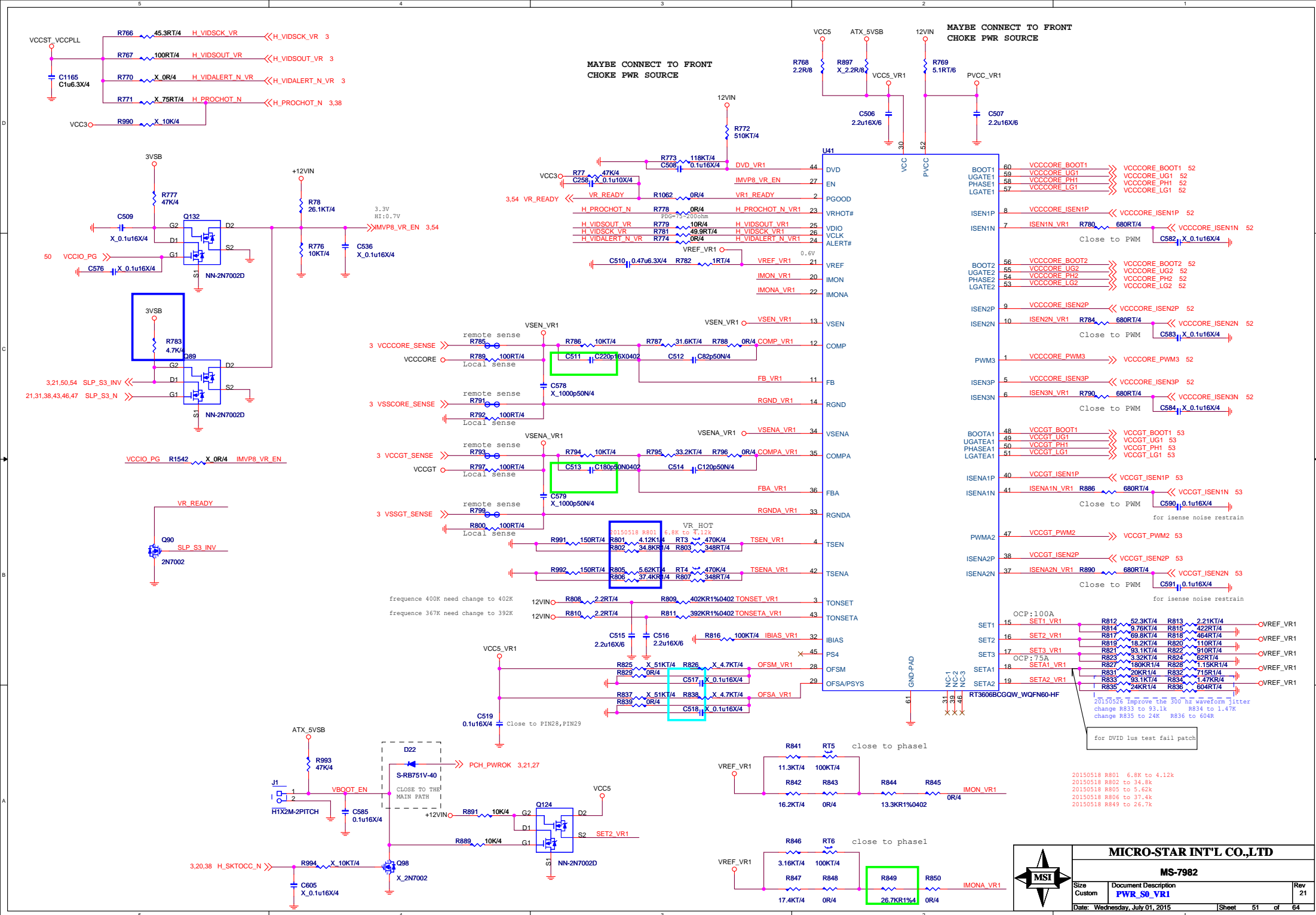


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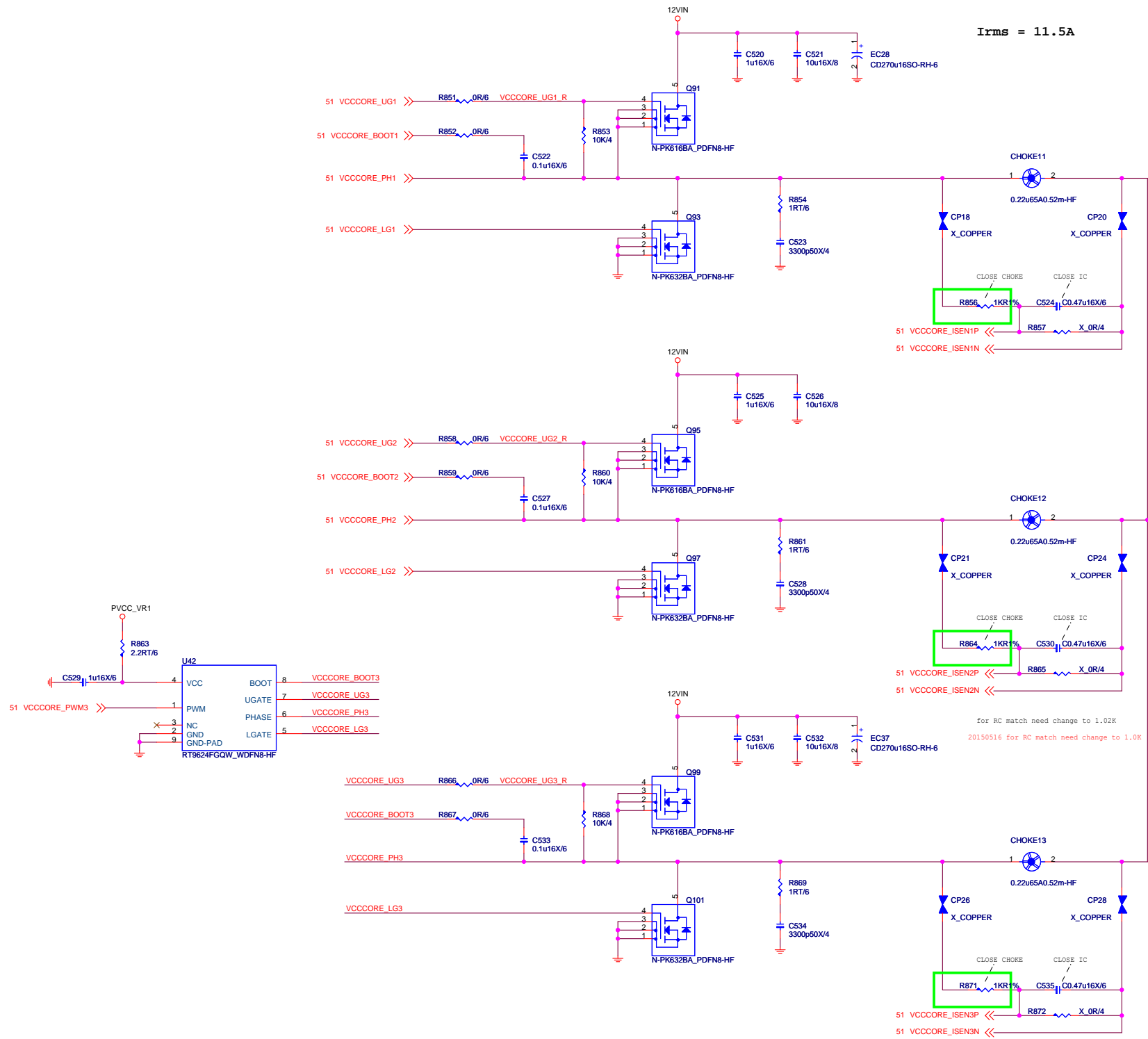
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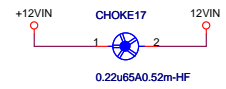
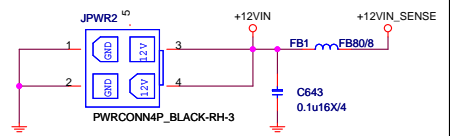
Size	Document Description
Custom	<b>PWR_S0_VR1</b>

	Rev 21
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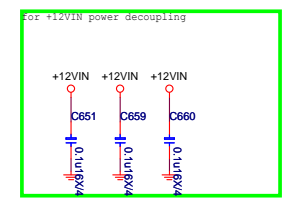
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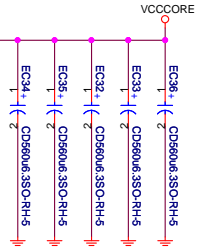
Irms = 11.5A



Total\_Irms = 24.1A



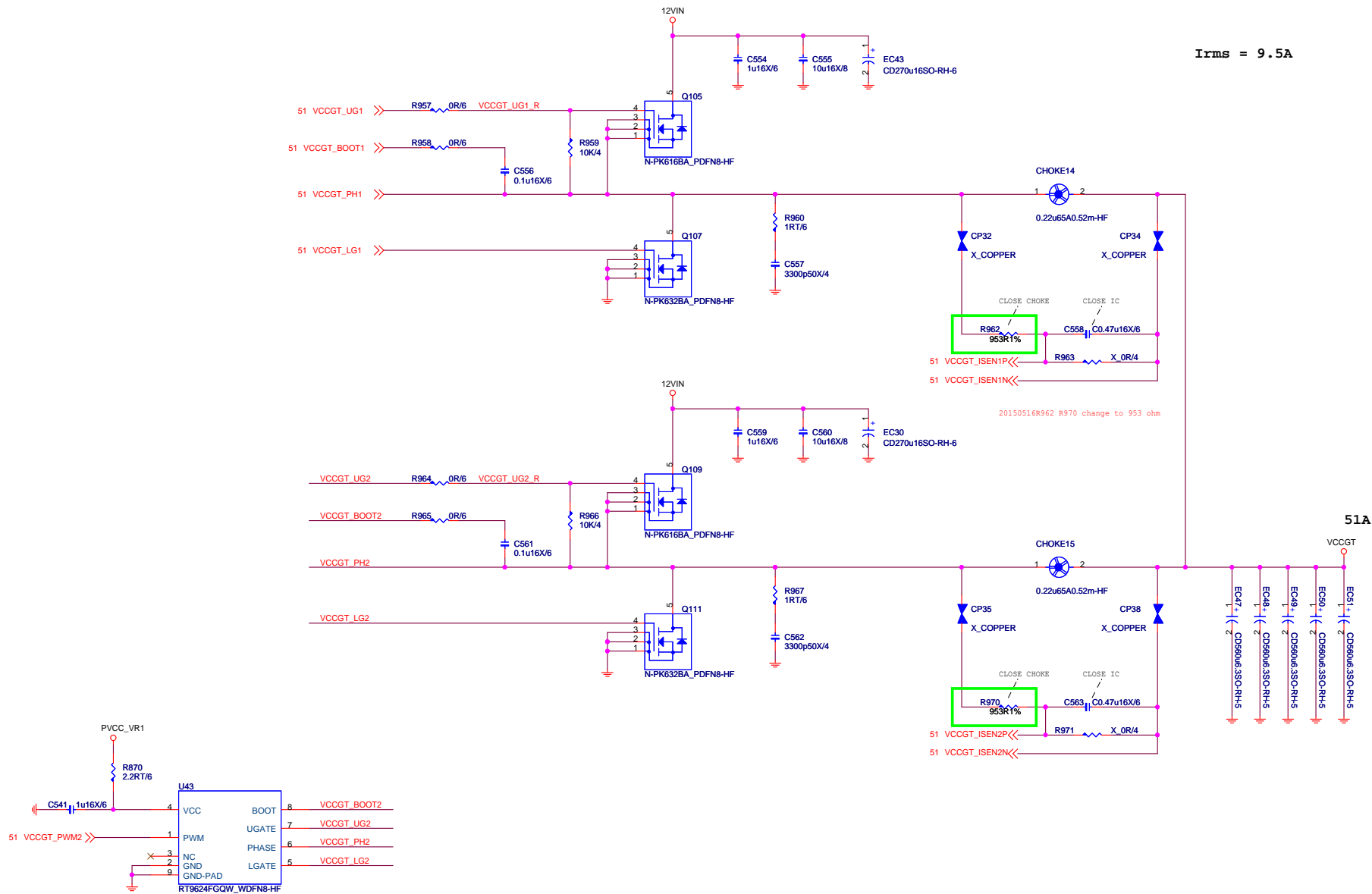
79A



for RC match need change to 1.02K  
20150516 for RC match need change to 1.0K



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I<sub>rms</sub> = 9.5A



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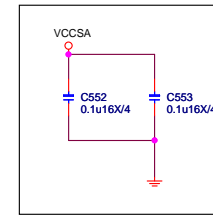
$$\begin{aligned} R_{ocs}(R15) &= OCP * R_{dson}(\text{Low side}) 3.3\text{mohm} / 10\mu A \\ &= 15.54 * (3.3)\text{mohm} / 10\mu A \\ &= 5.1282\text{Kohm} \end{aligned}$$

```
Rdson(low) 12V gate drive
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm
D03-3116M00-U47 : 2.5mohm
```

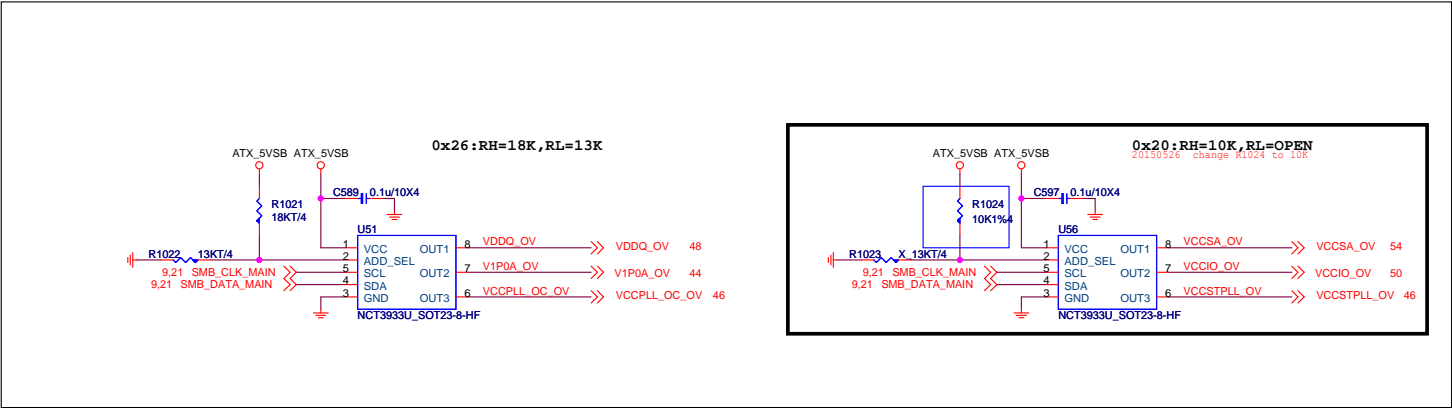
```

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
      = 11.1 * 0.4
      = 3.1A < 5000mA

```



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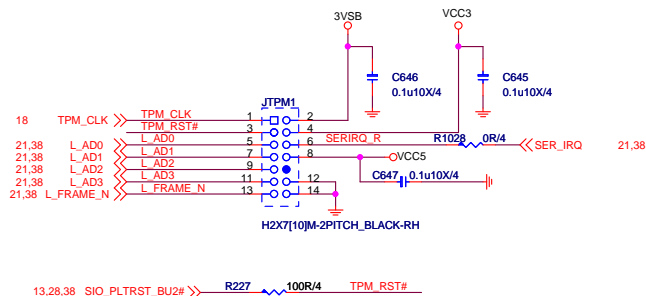


20150622 Remove Bottom LED

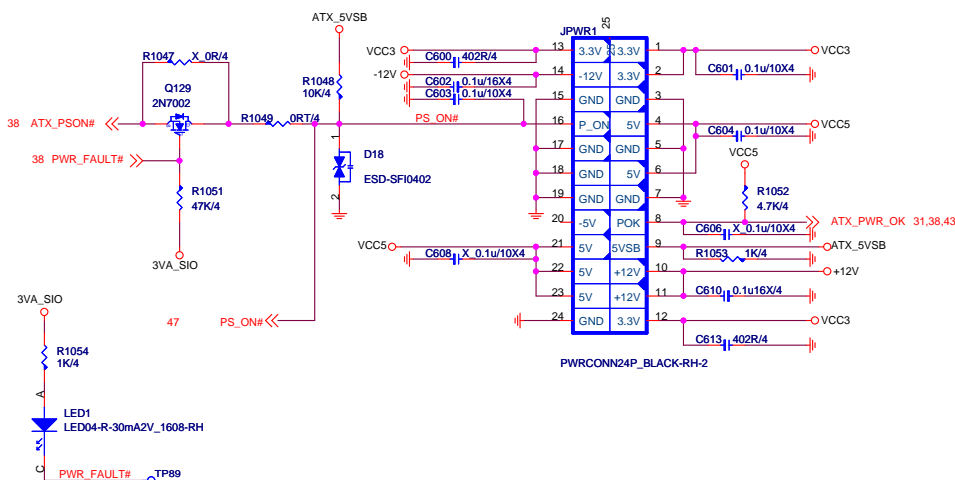
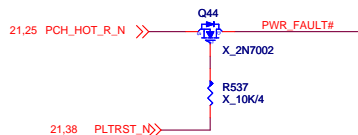


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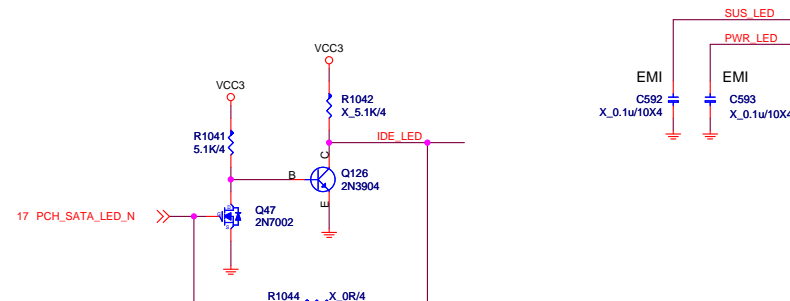
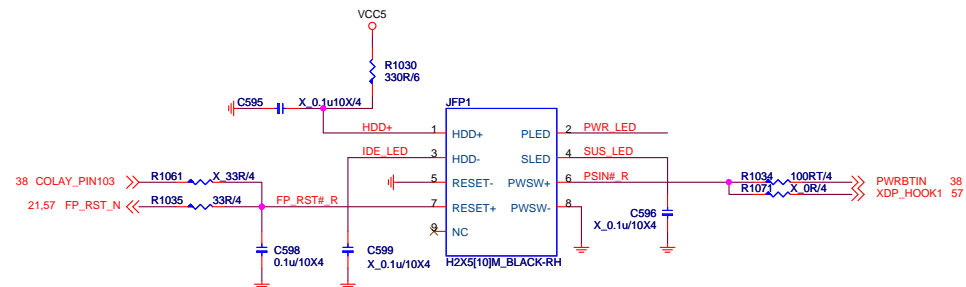
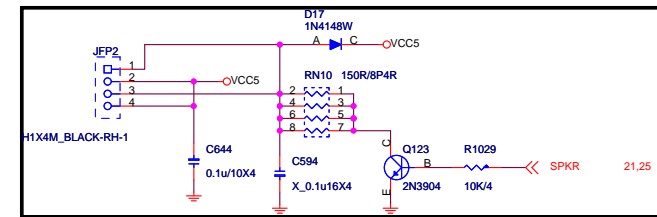
## TPM



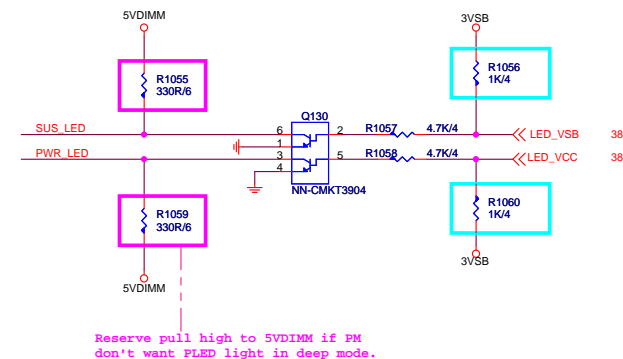
## ATX POWER CONNECTOR



## FRONT PANNEL



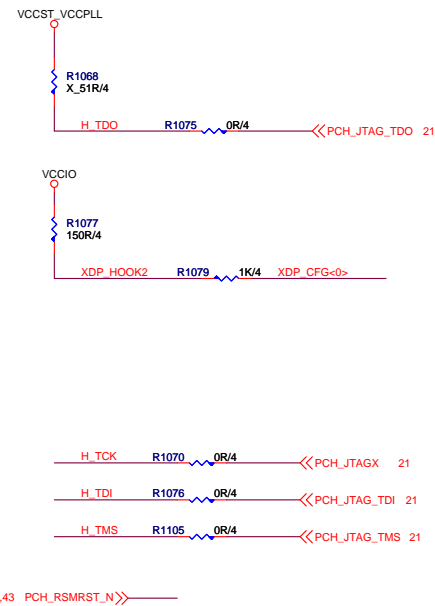
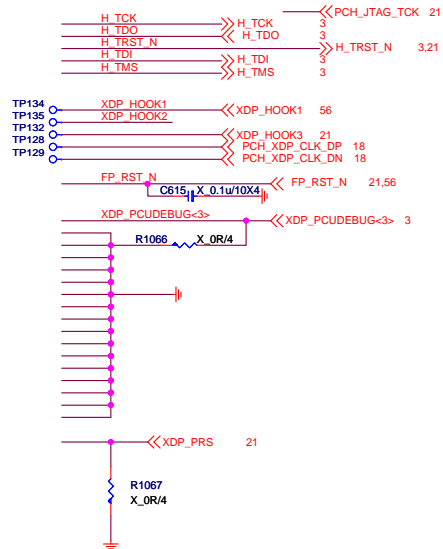
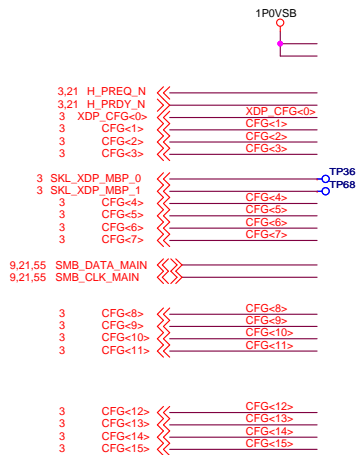
## LED ( for NCT6799D)



Reserve pull high to 5VDIMM if PM don't want PLED light in deep mode.

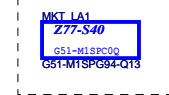
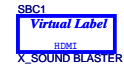
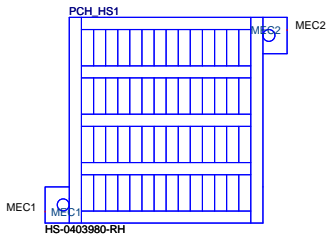


**Reserve debug port 5020**

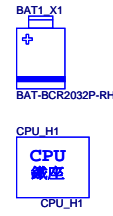


CLOSE TO PCH



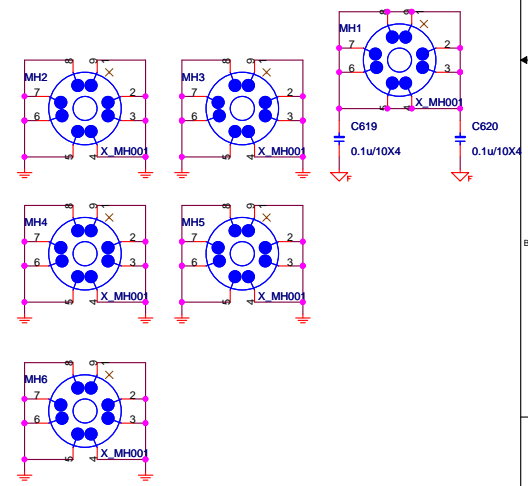


**PCH XDP PWRGD/RESET**

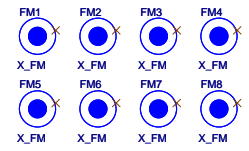


**Simulation**

**Mounting Holes**



**Optical Fiducial Marks-120**



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